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C	<div><h1>ZIDANE 2.0</h1><h2>www.aitech1.ru</h2><h3>MV Build</h3><h3>2011/03/03</h3></div>								C																																																																															
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F	<table><tr><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td></tr><tr><td>2011-02-09</td><td></td><td>B</td></tr><tr><td>2010-10-06</td><td>2010-EC0-020288</td><td>A</td></tr><tr><td>DATE</td><td>CHANGE NO.</td><td>REV</td></tr></table>																			2011-02-09		B	2010-10-06	2010-EC0-020288	A	DATE	CHANGE NO.	REV			<table><tr><td>EE</td><td>DATE</td><td>POWER</td><td>DATE</td></tr><tr><td>Chang, Tommy</td><td>2010-06-14</td><td>Ho, Wen-Pin</td><td>2010-06-14</td></tr><tr><td>DESIGN</td><td>Chang, Tommy</td><td>Ho, Wen-Pin</td><td>2010-06-14</td></tr><tr><td>CHECK</td><td>Chih, Johnson</td><td>Ho, Wen-Pin</td><td>2010-06-14</td></tr><tr><td>RESPONSIBLE</td><td>Chih, Johnson</td><td>Ho, Wen-Pin</td><td>2010-06-14</td></tr></table>	EE	DATE	POWER	DATE	Chang, Tommy	2010-06-14	Ho, Wen-Pin	2010-06-14	DESIGN	Chang, Tommy	Ho, Wen-Pin	2010-06-14	CHECK	Chih, Johnson	Ho, Wen-Pin	2010-06-14	RESPONSIBLE	Chih, Johnson	Ho, Wen-Pin	2010-06-14		<table><tr><td colspan="4">INVENTEC</td></tr><tr><td colspan="4">TITLE: ZIDANE2.0</td></tr><tr><td>SIZE =</td><td>3</td><td>VER :</td><td></td></tr><tr><td>FILE NAME :</td><td colspan="3">XXXX-XXXXXX-XX</td></tr><tr><td>P/N</td><td colspan="3">XXXXXXXXXXXX</td></tr></table>	INVENTEC				TITLE: ZIDANE2.0				SIZE =	3	VER :		FILE NAME :	XXXX-XXXXXX-XX			P/N	XXXXXXXXXXXX				<table><tr><td>SIZE</td><td>CODE</td><td>DOC. NUMBER</td><td>REV</td></tr><tr><td>A3</td><td>CS</td><td>I310A24024-0-MTR</td><td>B</td></tr><tr><td>SHEET</td><td>1</td><td>OF</td><td>58</td></tr></table>	SIZE	CODE	DOC. NUMBER	REV	A3	CS	I310A24024-0-MTR	B	SHEET	1	OF	58	F
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SHEET	1	OF	58																																																																																					
	1	2	3	4	5	6	7	8																																																																																

## Index

### PAGE

01. PROJECT NAME
02. INDEX
03. Block Diagram
04. POWER Procedure
05. DC & CHARGE Circuit
06. Battery CONN
07. +V3A & +V5A
08. +V1.5 & +V0.75
09. +V1.8S & +V1.05S
10. +VCC\_CORE
11. +VGFX\_CORE
12. VTT & VPCIE & VDDC\_GPU
13. +V5S & +V3S
14. CLK GEN
15. CPU-1
16. CPU-2
17. CPU-3
18. CPU-4
19. CPU-5
20. CPU-6
21. Thermal, Fan & XDP
22. DDR3-1
23. DDR3-2
24. PCH-1
25. PCH-2
26. PCH-3
27. PCH-4
28. PCH-5
29. PCH-6
30. PCH-7

### PAGE

31. PCH-8
32. PCH-9
33. KBC
34. Keyboard & TouchPad
35. CRT CONN
36. LCM CONN
37. HDMI CONN
38. SATA HDD & ODD
39. LAN
40. RJ-45
41. Card Reader
42. Audio Codec
43. HP JACK & MIC JACK
44. ESATA, SCREW
45. WLAN & BlueTooth
46. USB, PowerButton(DB)
47. WWAN(Optional)
48. FP & HD LOCK(Optional)
49. PARK-S3 PCIE INTERFACE
50. PARK-S3 Display and GIPO INTERFACE
51. PARK-S3 CLK and DDC INTERFACE
52. PARK-S3 POWER INTERFACE
53. PARK-S3 DP Power and LVDS INTERFACE
54. PARK-S3 Memory INTERFACE
55. VRAM-1(DDR3)
56. VRAM-2(DDR3)

**INVENTEC**

TITLE			
ZIDANE2.0			
Index			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B
SHEET		2	OF 58

CHANGE by *Drawer Name* 9-Feb-2011

1 2 3 4 5 6 7 8

A

B

C

D

E

F

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**DIS ONLY**

Discrete Graphic  
**ATI Seymour S3**  
P49~54

DDR III VRAM 64M X 16  
DDR III VRAM 64M X 16  
DDR III VRAM 64M X 16  
DDR III VRAM 64M X 16

**Sandy Bridge**  
(Socket-rPGA989)  
37.5mm x 37.5mm  
P15~20

DDR3  
DDR3

**DDR3 SO-DIMM 1**  
P22

**DDR3 SO-DIMM 2**  
P23

**COUGAR POINT**  
25mm x 25mm

HDMI  
VGA  
LVDS  
PCIE  
PCIE  
PCIE  
SATA  
SATA

**HDMI**  
P37

**CRT**  
P35

**LCM**  
P36

**ATHEROS GLAN**  
P39

**RJ-45**  
P40

**CARD READER minicard**  
P41

**TI TUSB7320**  
P57

**SATA ODD**  
P38

**SATA HDD**  
P38

**SPKR**  
P42

**HP JACK**  
P43

**MIC JACK**  
P43

**int DMIC**  
P36

**IDT 92HD80 AudioCodec**  
P42

**ITE IT8518E KBC**  
P33

**SPI ROM 4MB BIOS**  
P24

**SPI ROM EC FW 512KB (BIOS)**  
P33

**Keyboard**  
P34

**Touchpad**  
P34

**USB 8 WLAN+BT**  
P45

**USB 3 WWAN minicard**  
P47

**USB 0 USB3.0 CONN.**  
P58

**USB 5 Webcam**  
P36

**USB 1 USB CONN01**  
P44

**USB 9 USB CONN02**  
P44

**USB 10 Bluetooth**  
P45

**USB 11 FingerPrint**  
P48

**MAIN BATT**  
P06

**System Charger DC / DC System Power**  
P05

**Thermal meter TI TMP431B**  
P51

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INVENTEC				
TITLE ZIDANE2.0 Block Diagram				
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SHEET		3	OF 58	

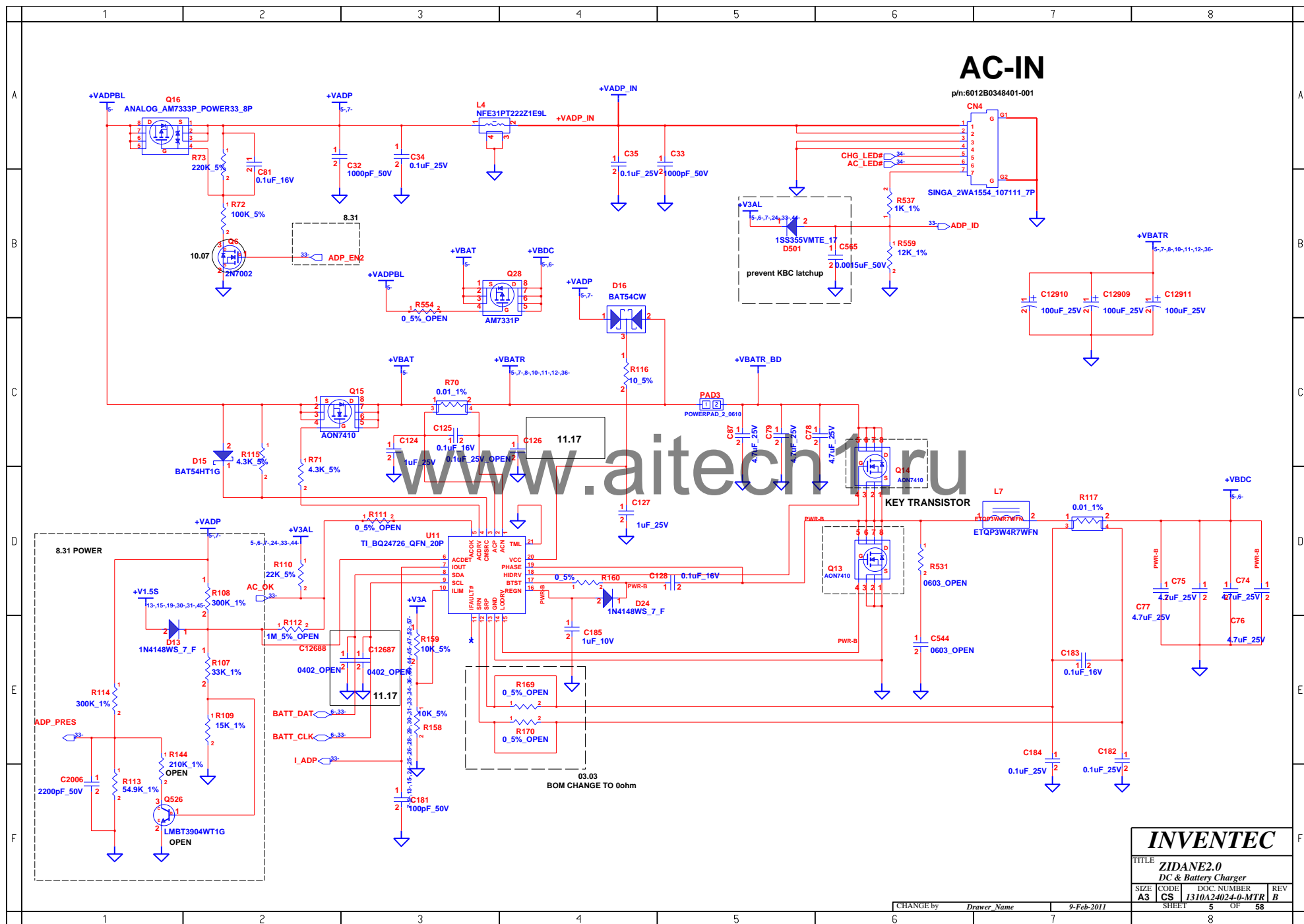
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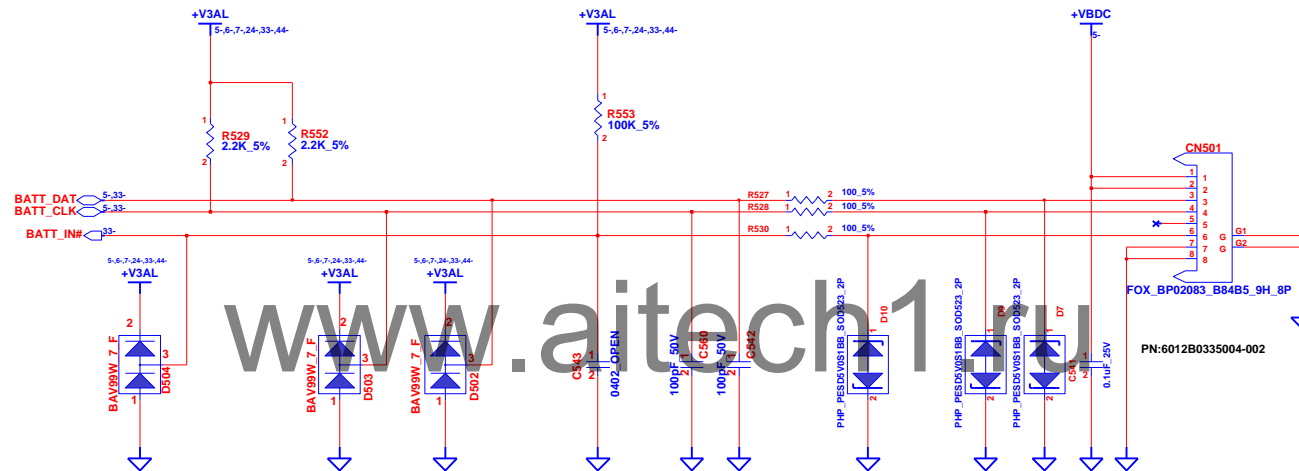
1 2 3 4 5 6 7 8

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SIZE	CODE	DOC. NUMBER	REV
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SHEET		3	OF 58

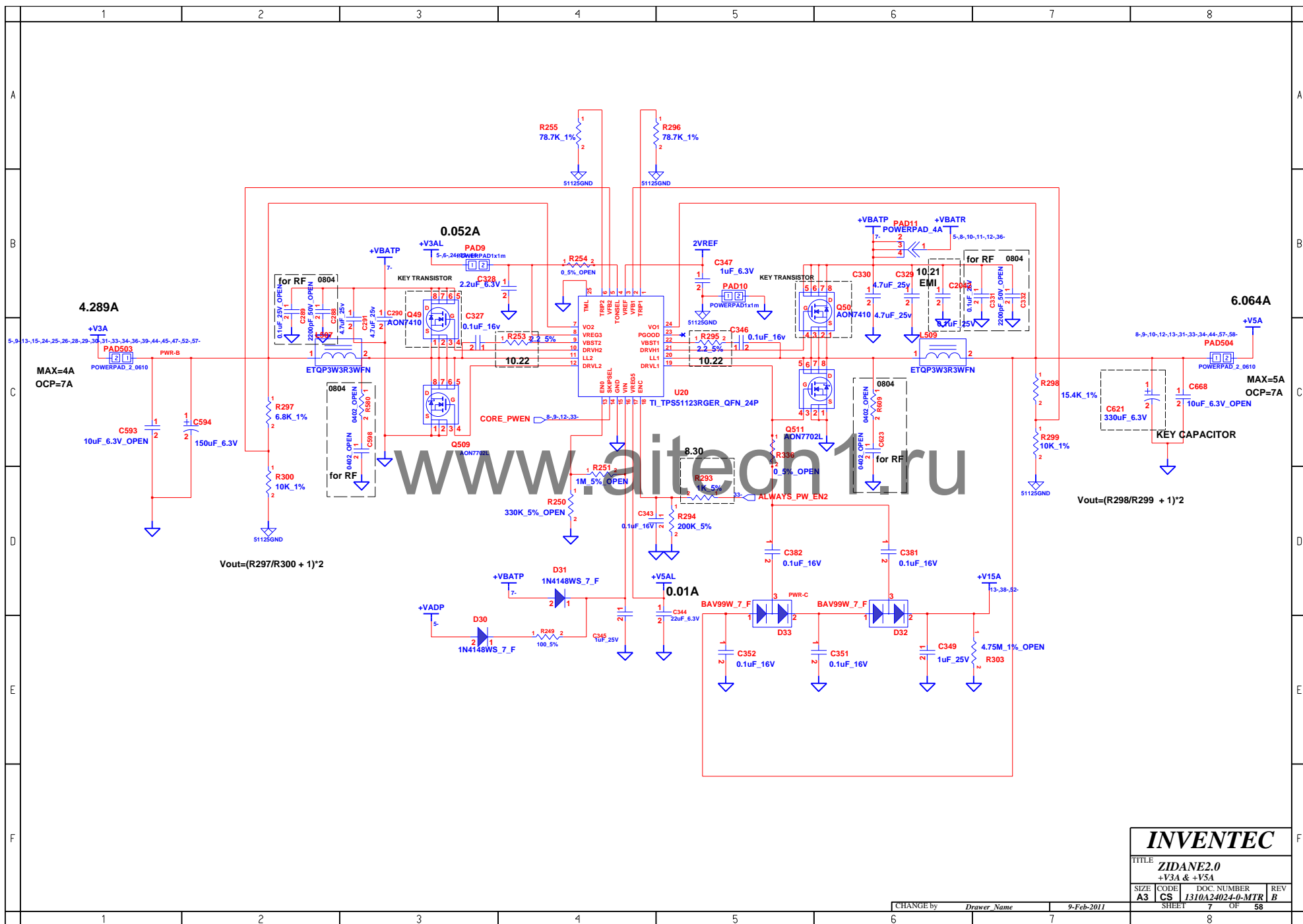
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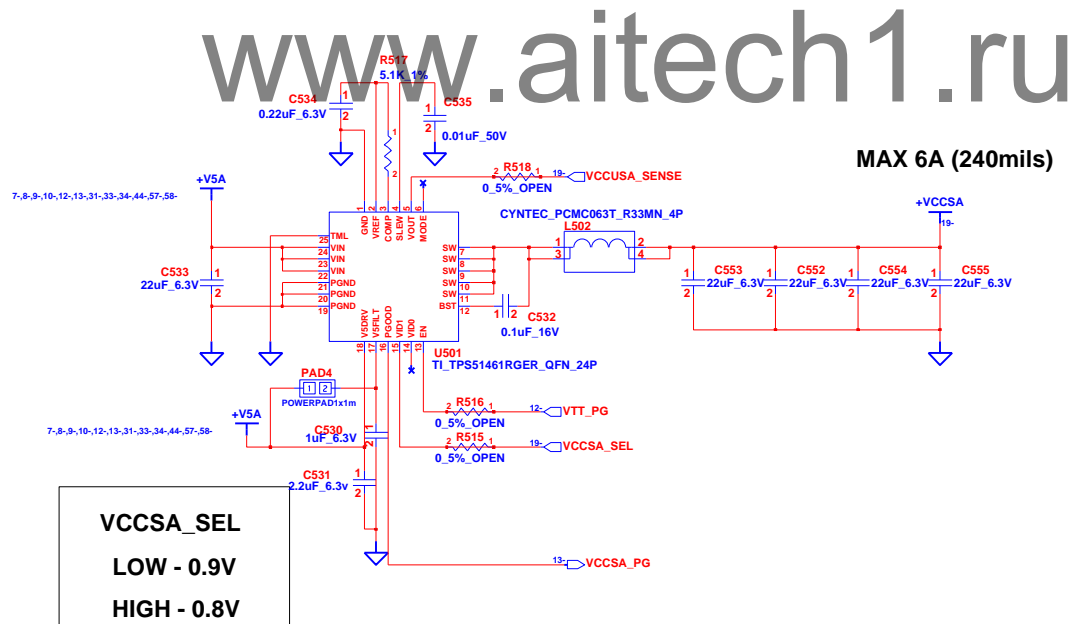
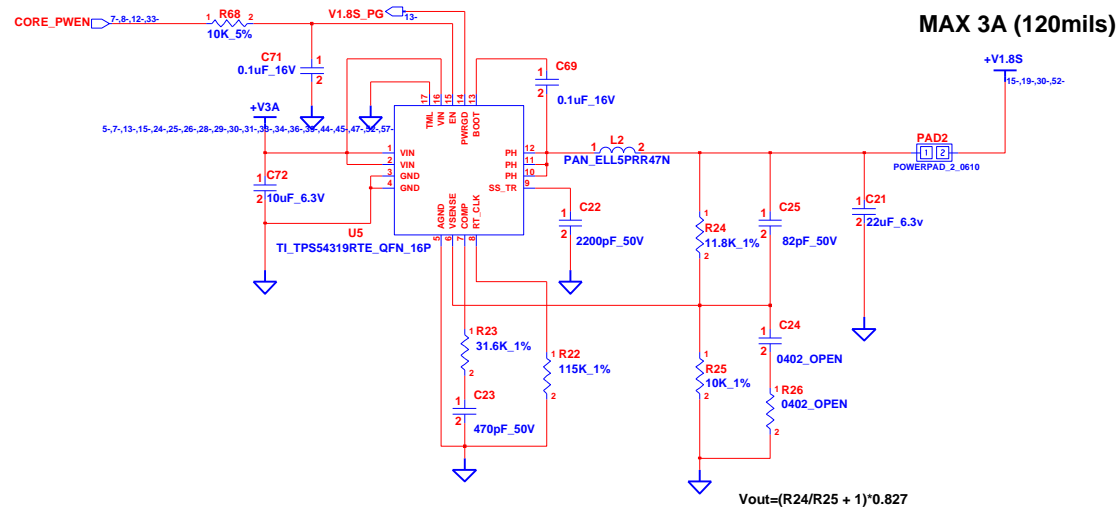


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ZIDANE2.0			
Battery CONN			
SIZE	CODE	DOC. NUMBER	REV
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SHEET		6	OF 58









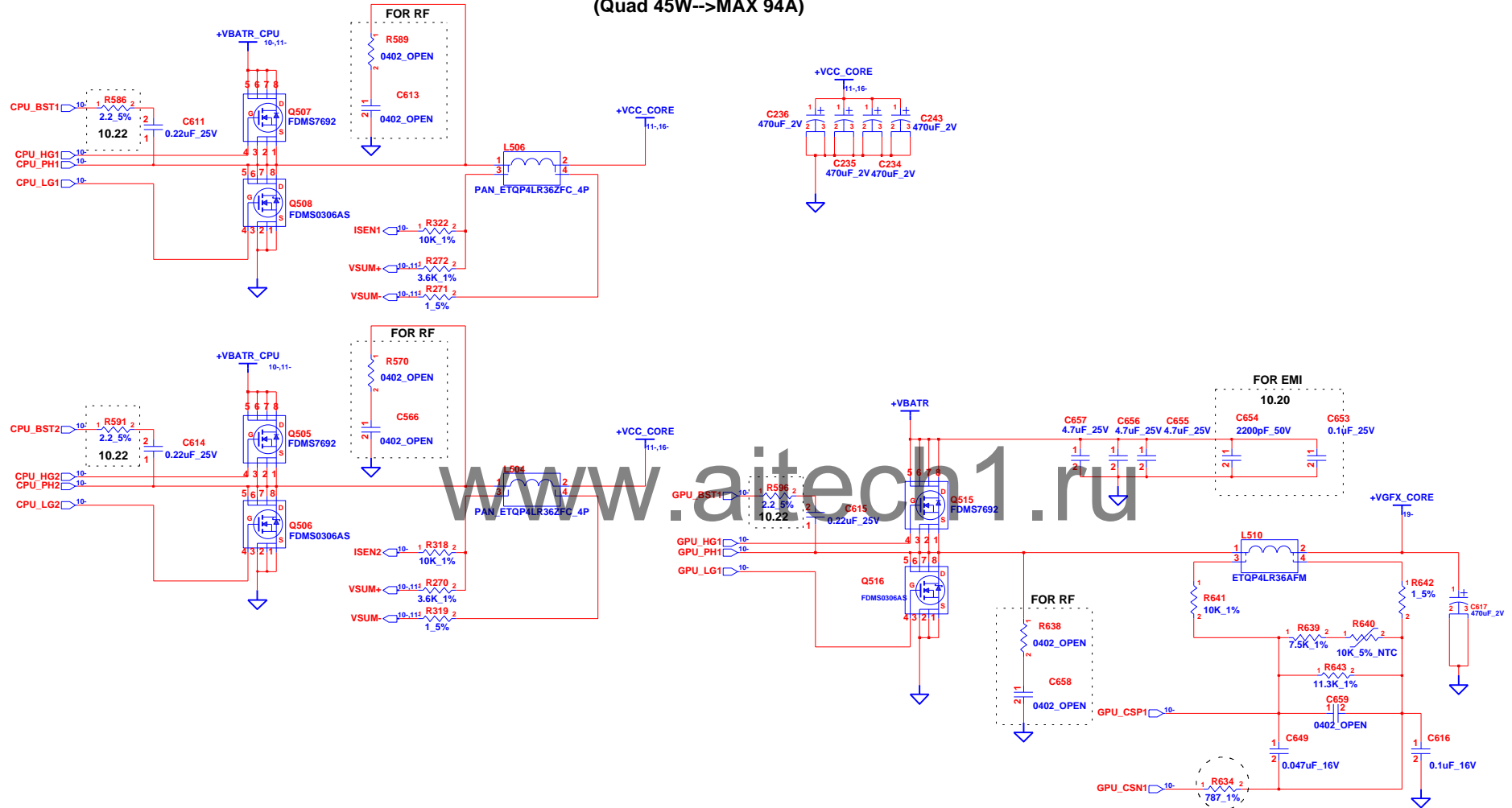
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TITLE			
ZIDANE2.0			
+V1.8S & +VCCSA			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B
SHEET		9	OF 58

CHANGE by *Drawer Name* 9-Feb-2011



VCC\_CORE (SV 35W-->MAX 53A)  
(Quad 45W-->MAX 94A)

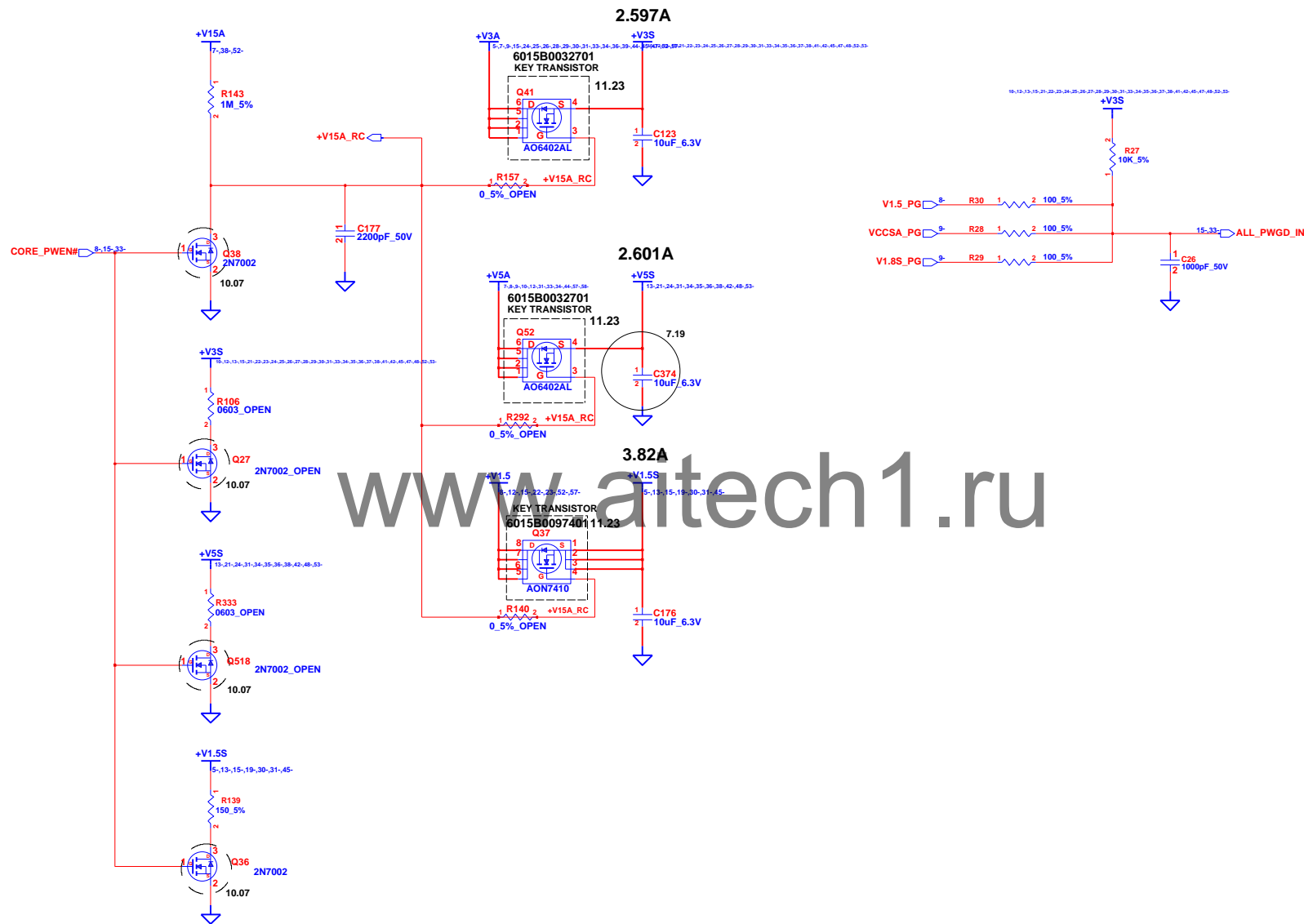


**INVENTEC**

TITLE			
ZIDANE2.0			
+VGFX_CORE			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B
SHEET		11	OF 58

CHANGE by *Drawer Name* 9-Feb-2011





# INVENTEC

TITLE			
ZIDANE2.0			
+V5S & +V3S			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B
SHEET		13	OF 58

CHANGE by *Drawer Name* 9-Feb-2011

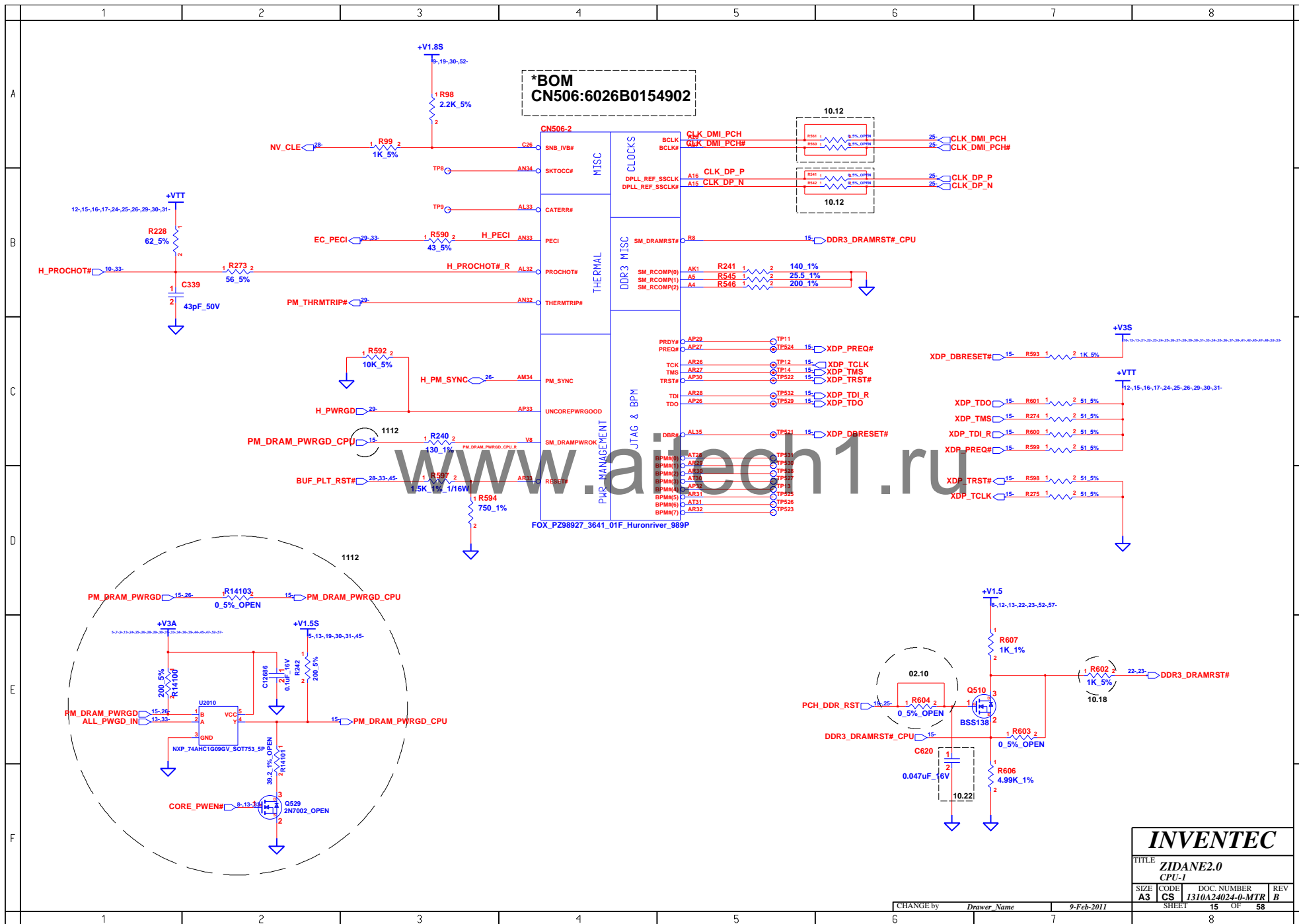
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A									A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

BLANK

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INVENTEC			
TITLE ZIDANE2.0 CLK GEN			
SIZE A3	CODE CS	DOC. NUMBER 1310A24024-0-MTR	REV B
SHEET 14		OF 58	

CHANGE by Drawer Name 9-Feb-2011



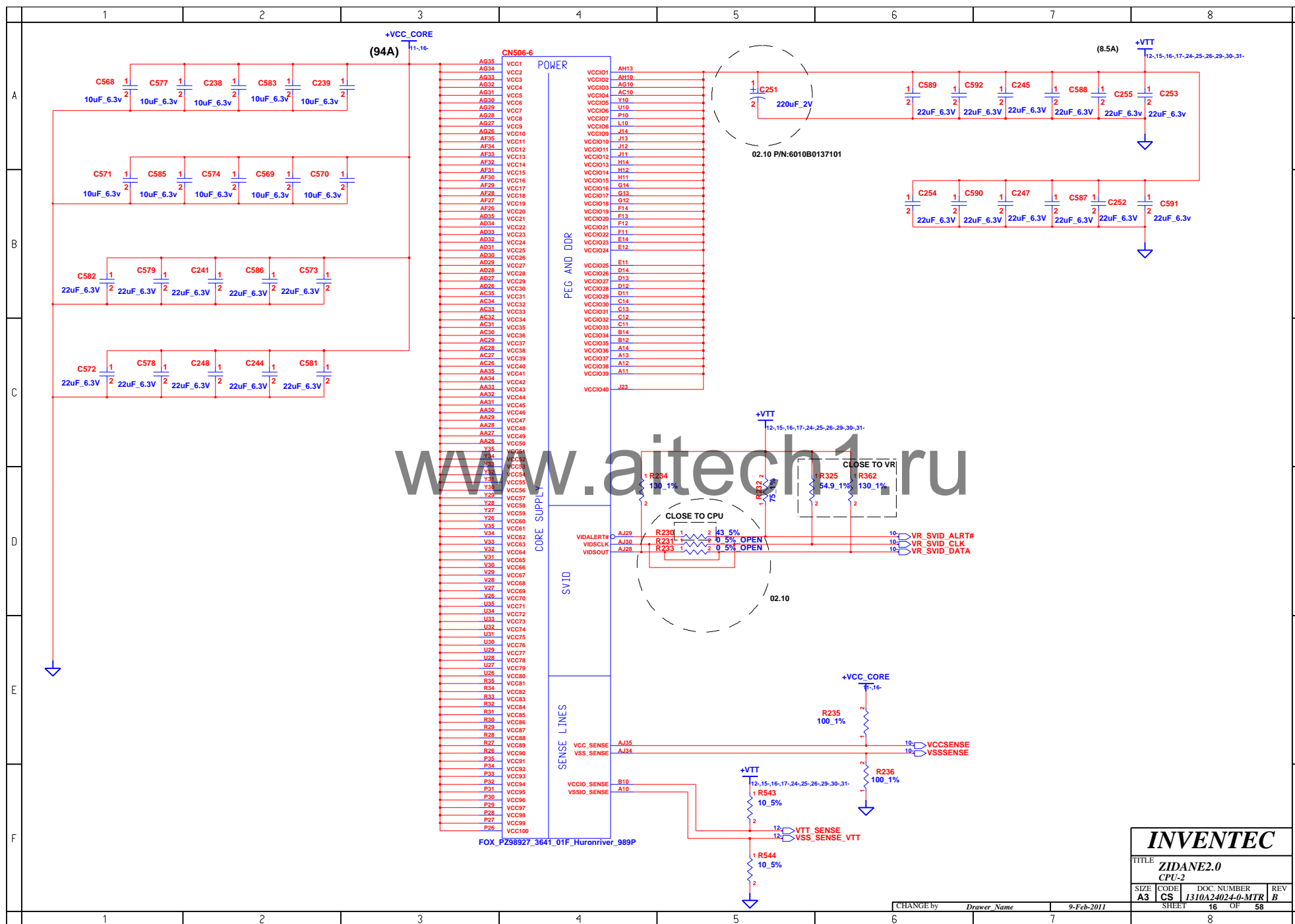
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TITLE  
**ZIDANE2.0**  
**CPU-1**

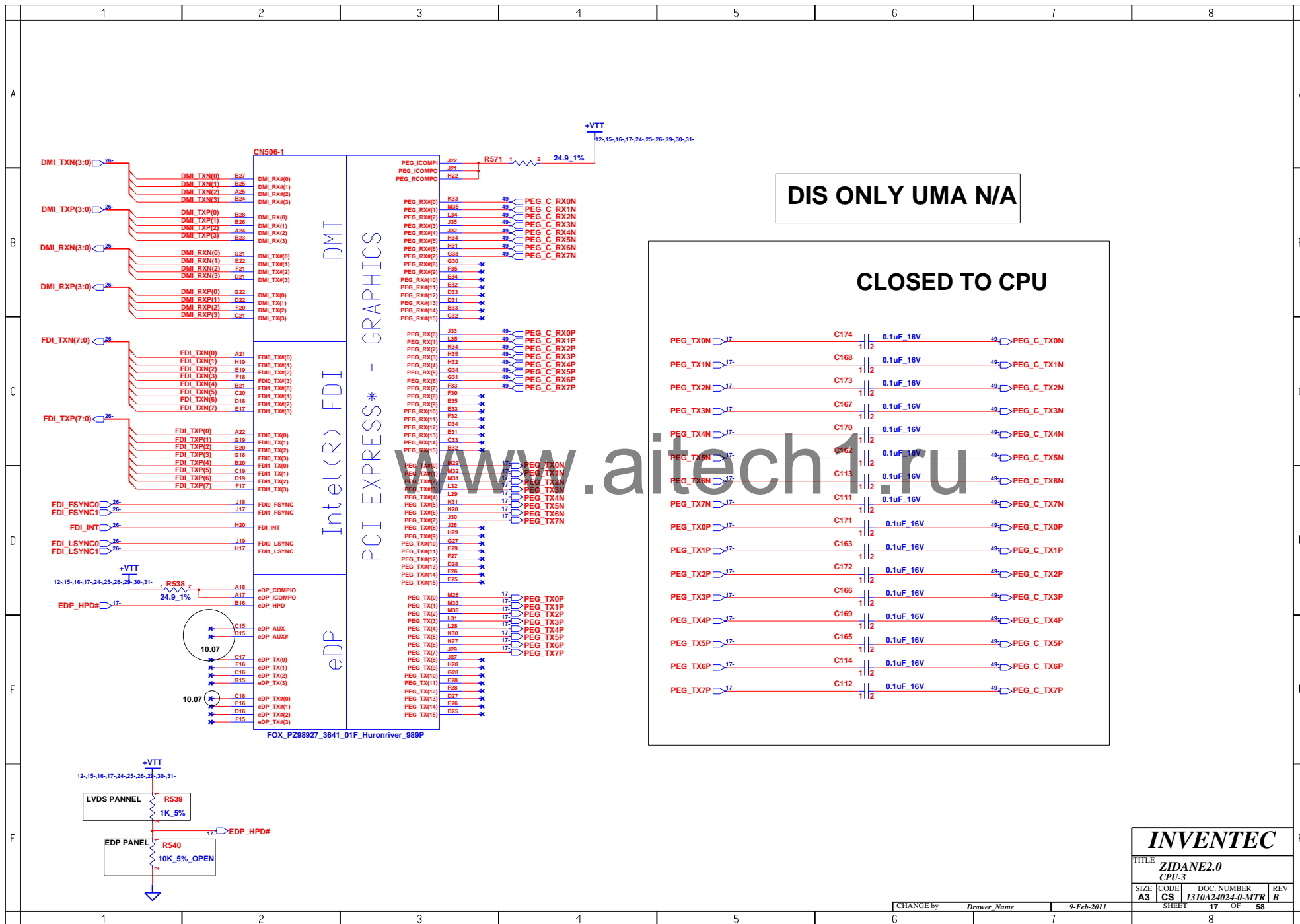
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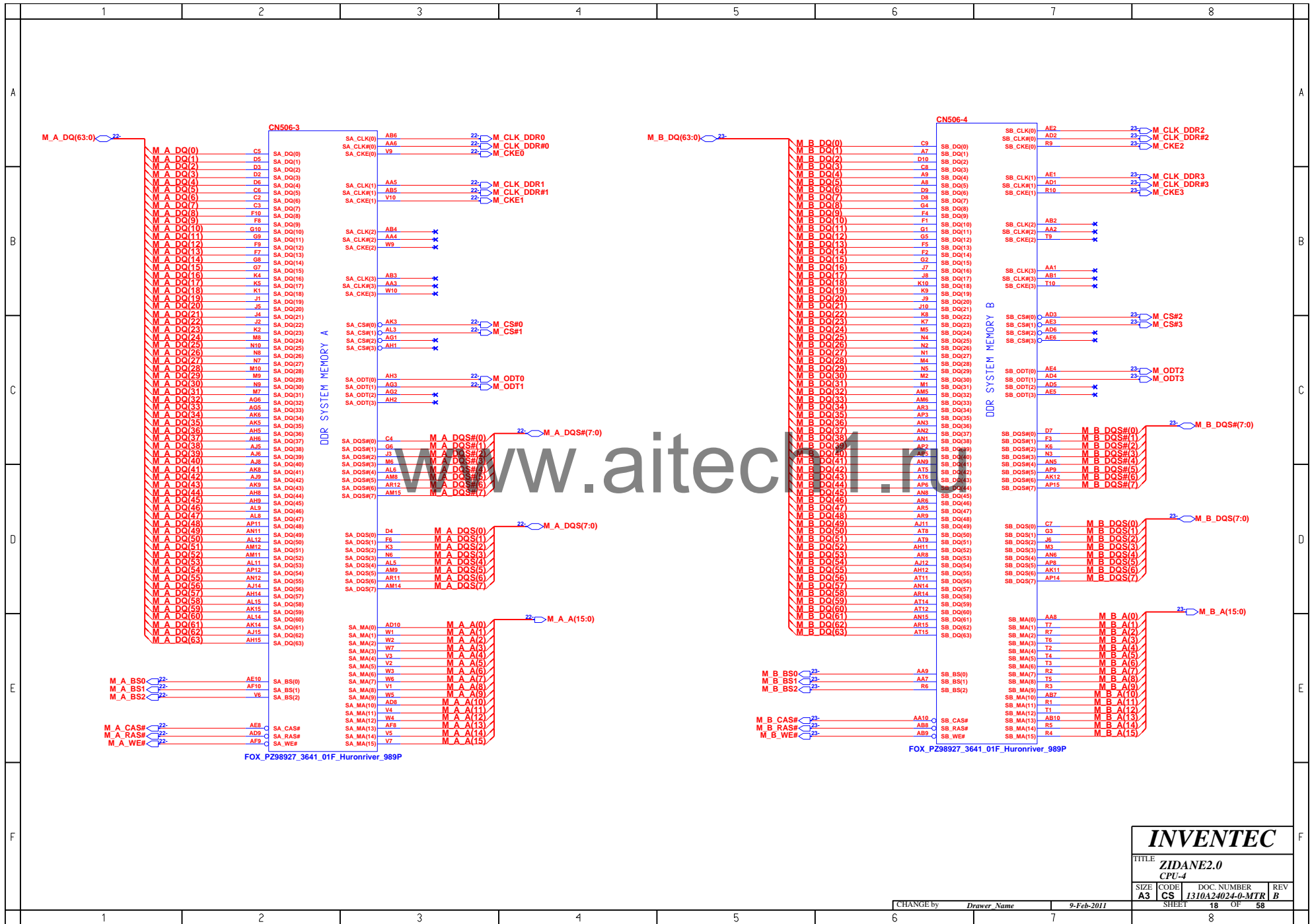
CHANGE by *Drawer Name* 9-Feb-2011

SHEET 15 OF 58





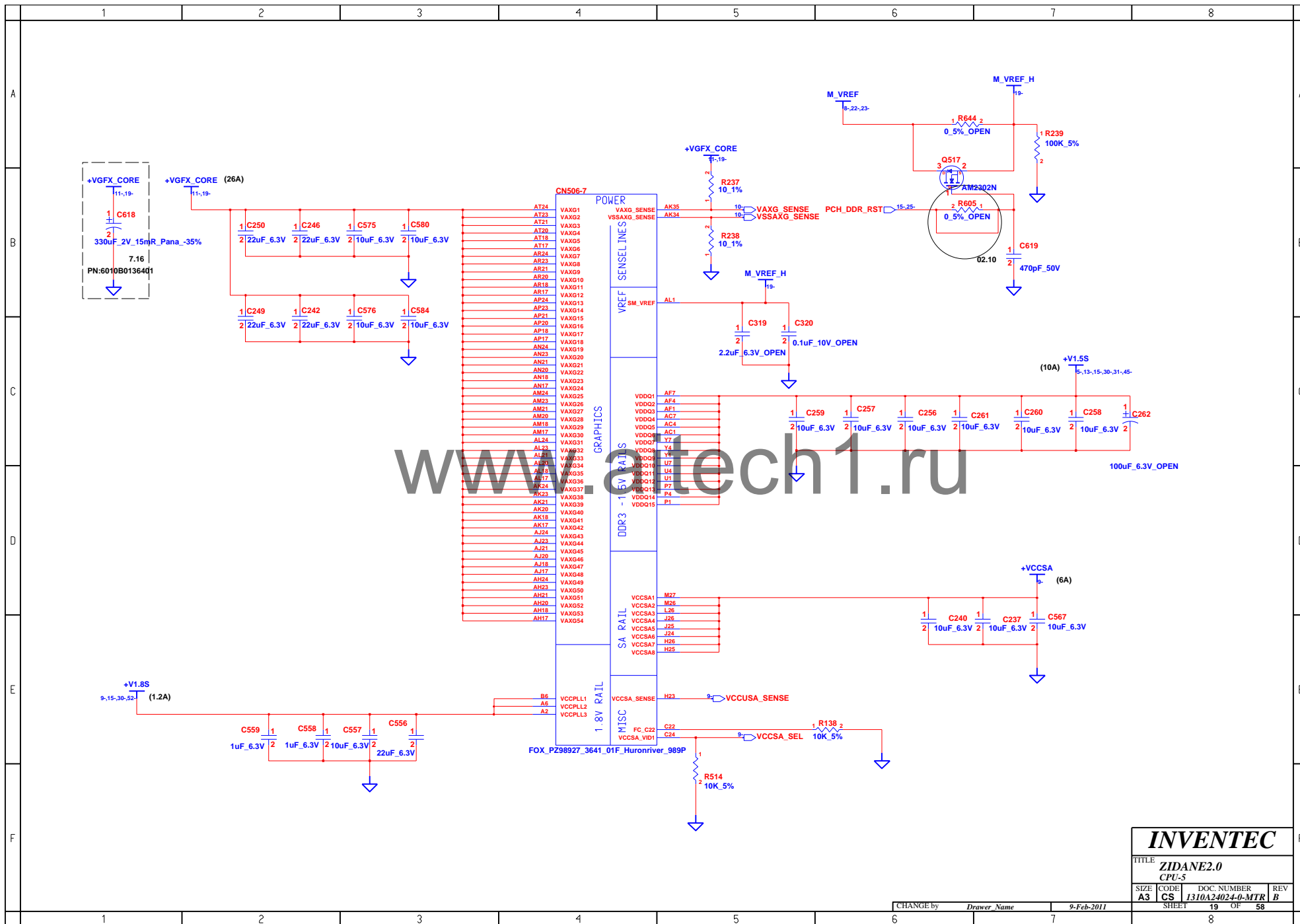




**INVENTEC**

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ZIDANE2.0			
CPU-4			
SIZE	CODE	DOC. NUMBER	REV
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SHEET		18	OF 58

CHANGE by Drawer Name 9-Feb-2011



**INVENTEC**

TITLE			
ZIDANE2.0			
CPU-5			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B

CHANGE by: Drawer Name 9-Feb-2011

SHEET 19 OF 58





## KEY IC

\*BOM  
U502 : 6019B0843501

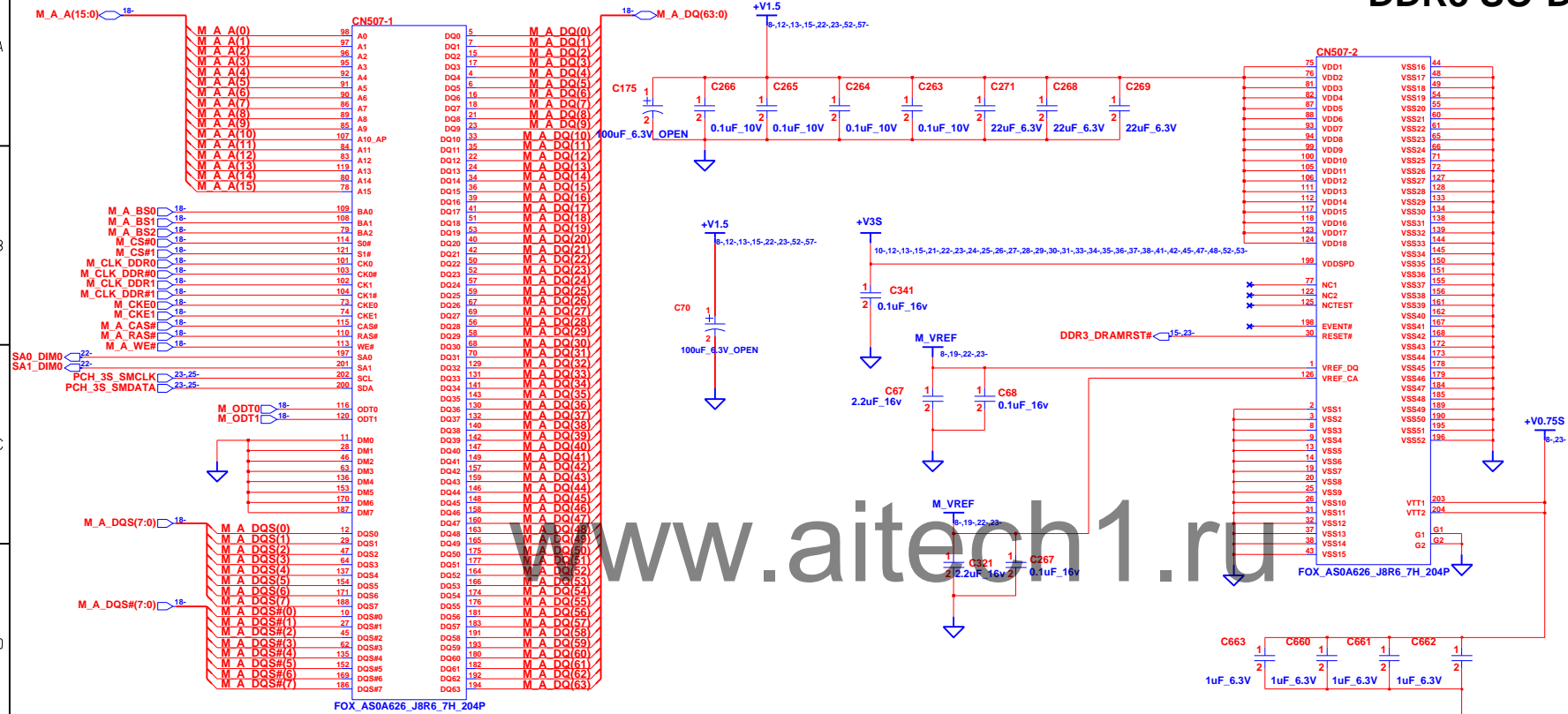
TEMPERATURE SETTING IS 80 DEGREE C

TITLE			
<b>ZIDANE2.0</b> <i>Thermal, Fan &amp; XDP</i>			
SIZE	CODE	DOC. NUMBER	REV
<b>A3</b>	<b>CS</b>	<b>1310A24024-0-MTR</b>	<b>B</b>
SHEET		21	OF 58

CHANGE by	<i>Drawer_Name</i>	9-Feb-2011
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SHEET	21
	8

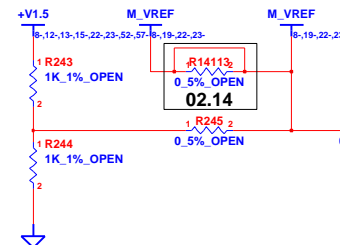
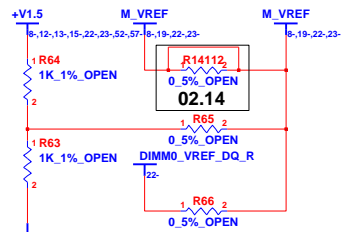
# DDR3 SO-DIMM 1



## NOTE:

IF SA0\_DIM0=0, SA1\_DIM0=0  
SO-DIMMA SPD ADDRESS IS 0xA0  
SO-DIMMA TS ADDRESS IS 0x30

IF SA0\_DIM0=1, SA1\_DIM0=0  
SO-DIMMA SPD ADDRESS IS 0xA2  
SO-DIMMA TS ADDRESS IS 0x32



**INVENTEC**

TITLE: ZIDANE2.0  
DDR3-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B

CHANGE by: Drawer Name 9-Feb-2011

SHEET 22 OF 58

# DDR3 SO-DIMM 2

CN508(lower) : 6026B0121102  
\*BOM

Layout Note: Place  
these Caps near  
SO-DIMM1 power pin

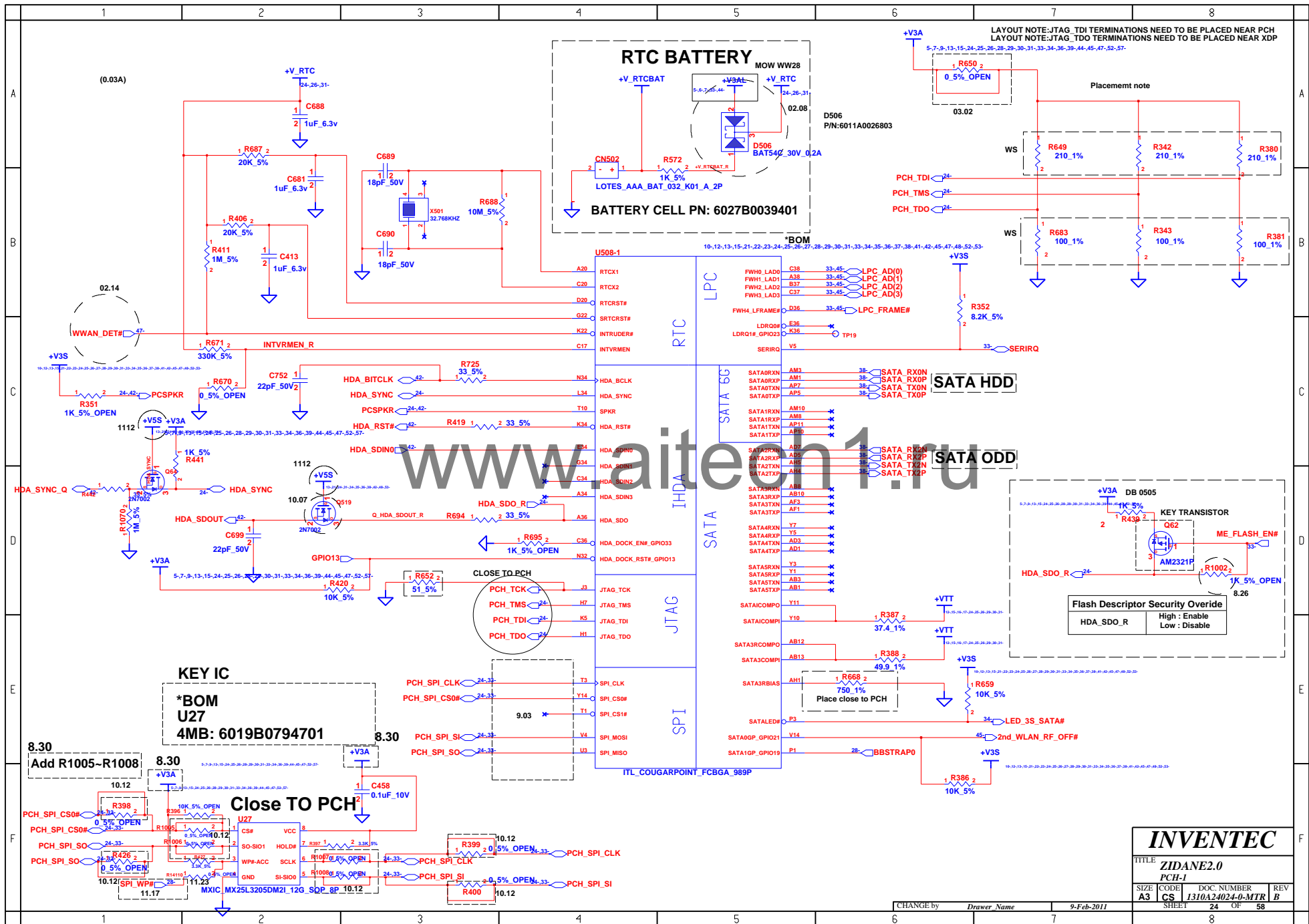
Place these caps  
close to VTT1 and  
VTT2

Place these caps  
close to VTT1 and  
VTT2

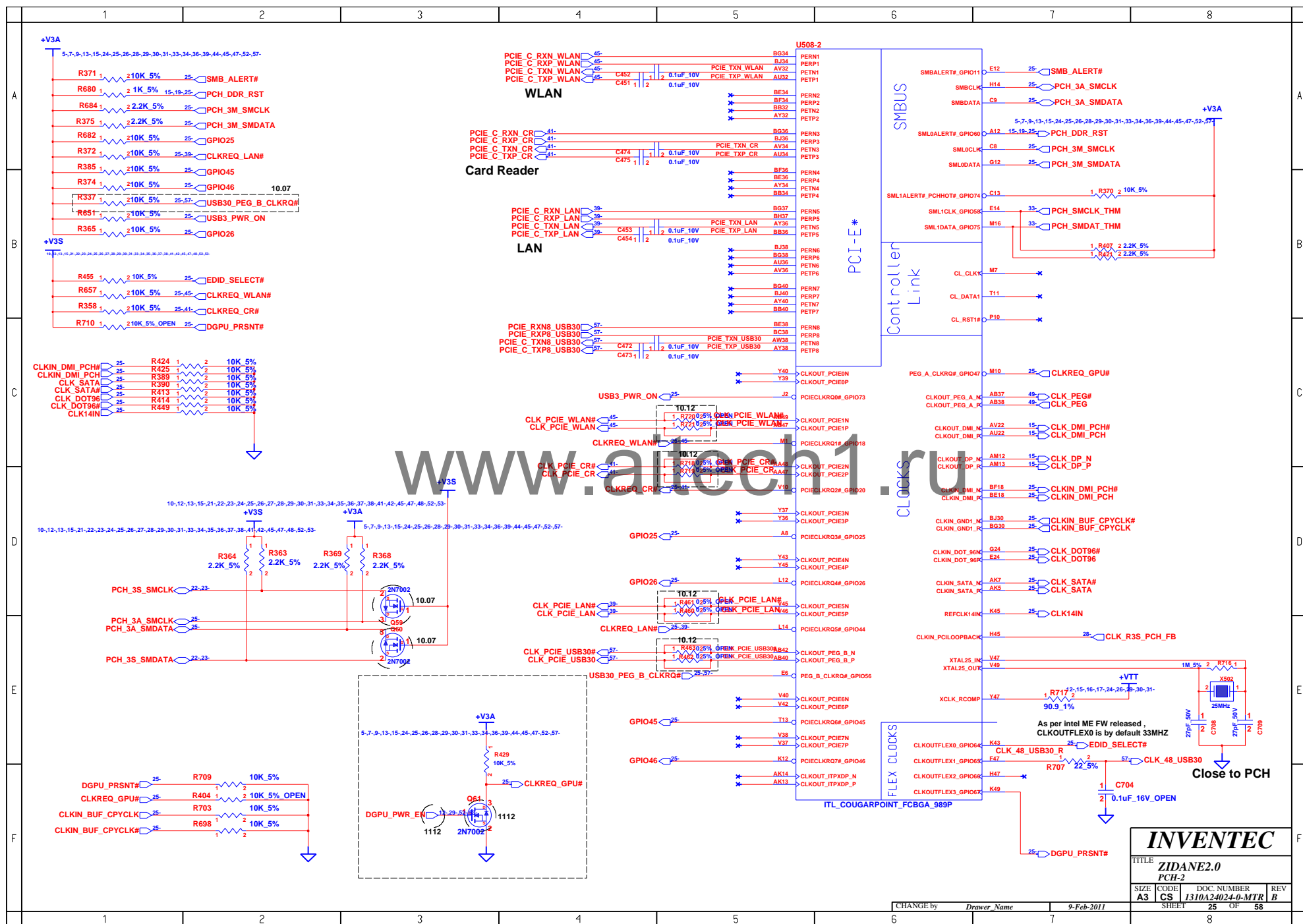
NOTE:  
SO-DIMM SPD ADDRESS IS 0xA4  
SO-DIMM TS ADDRESS IS 0x34

INVENTEC				
TITLE: ZIDANE2.0 DDR3-2				
SIZE A3	CODE CS	DOC. NUMBER 1310A24024-0-MTR	REV B	
CHANGE by		Drawer Name	9-Feb-2011	
SHEET		23	OF	58

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**Notes:**

- 1.SLP\_SUS and SUSACK# are NC if DSW is not supported
- 2.DPWROK should connect to RSMRST# if DSW is not supported
- 3.PCH\_DPWROK pull up to +V3S enables DSW support. No install R5261 to disable DSW

**System Power Management**

**U508-3**

**DMI**

**FDI**

**System Power Management**

**ITL COUGARPOINT\_FCBGA\_989P**

**INVENTEC**

**TITLE** ZIDANE2.0  
PCH-3

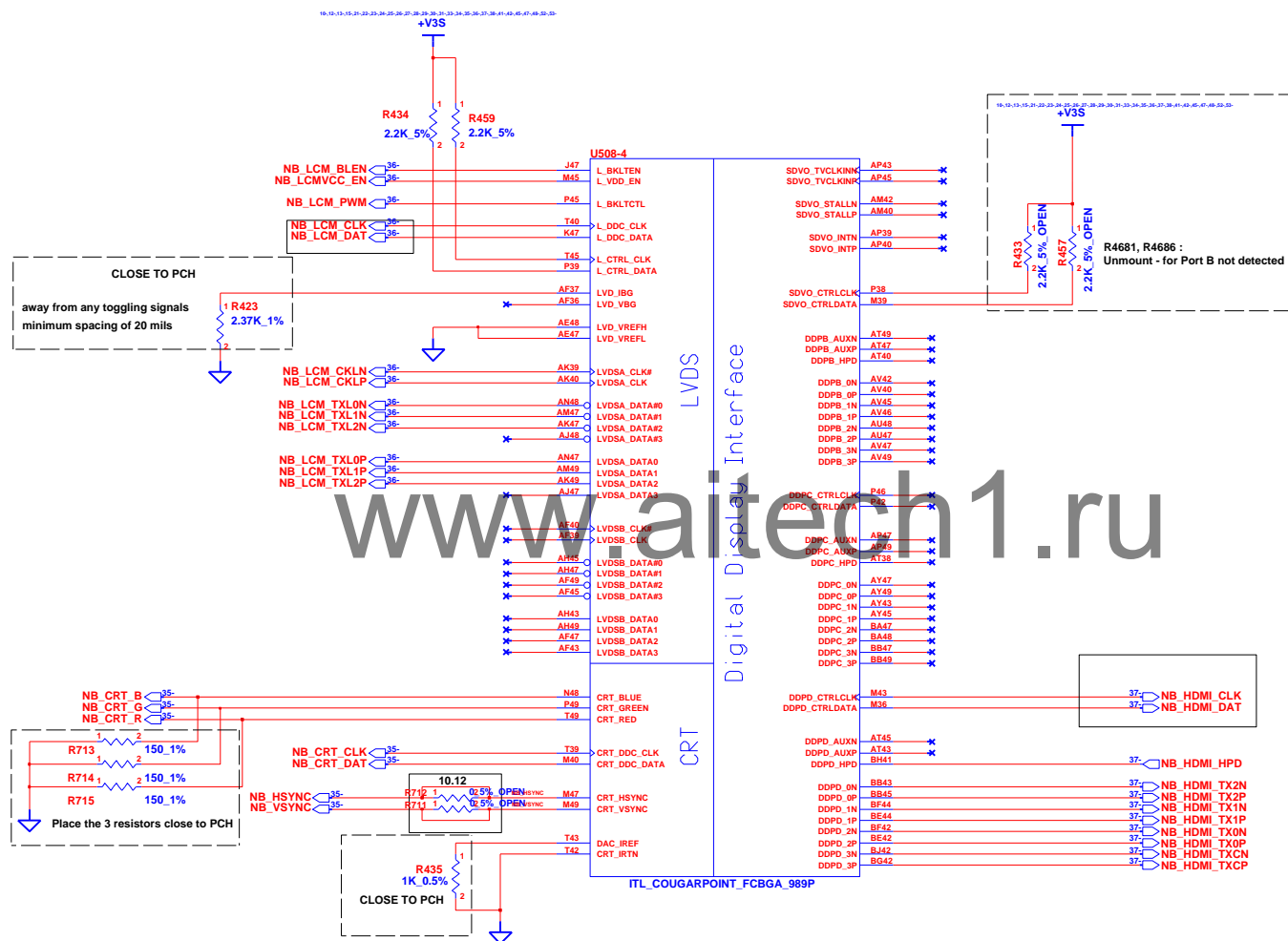
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**SHEET** 26 **OF** 58

**CHANGE by** *Drawer Name* **9-Feb-2011**

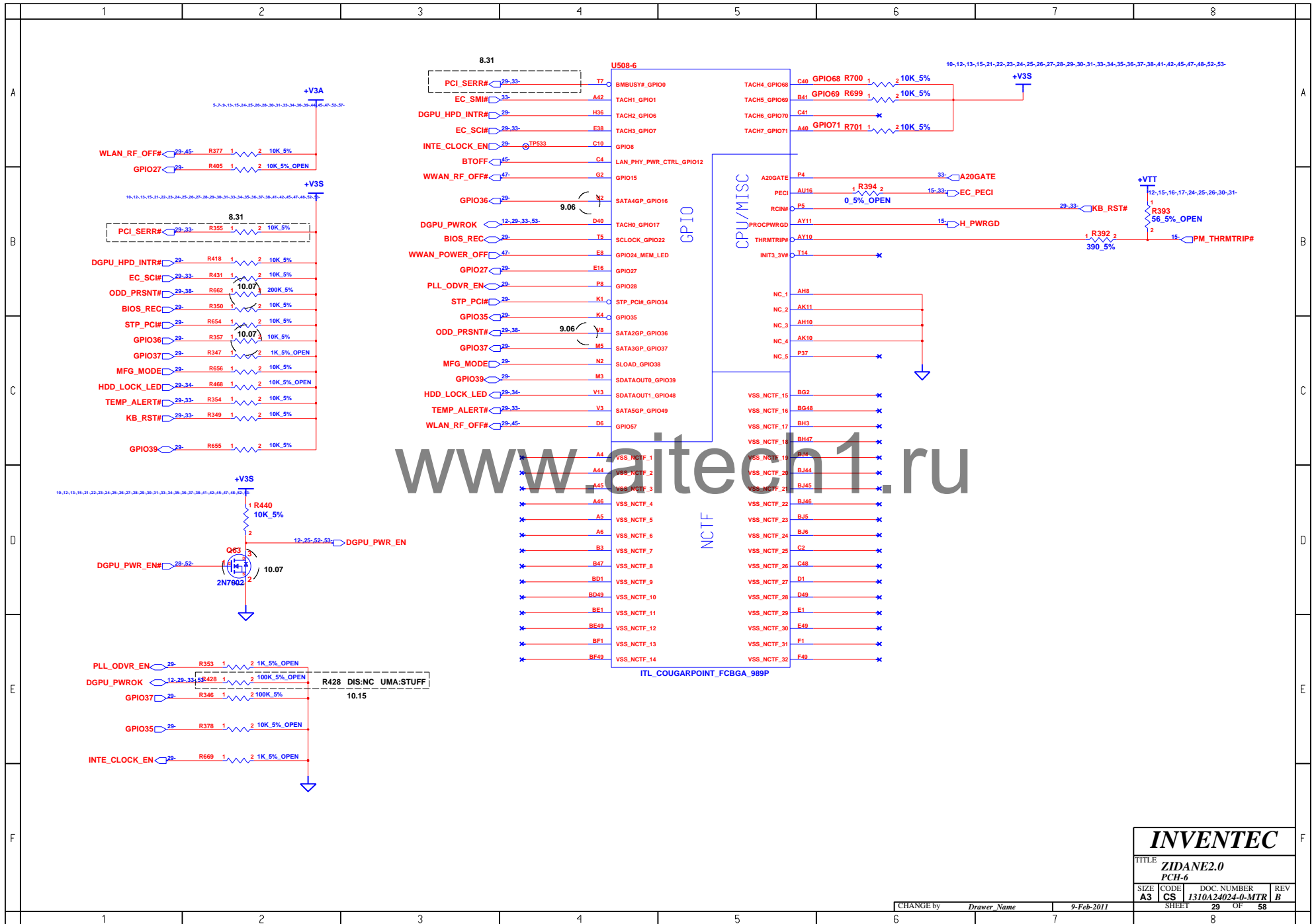
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SHEET		26	OF 58

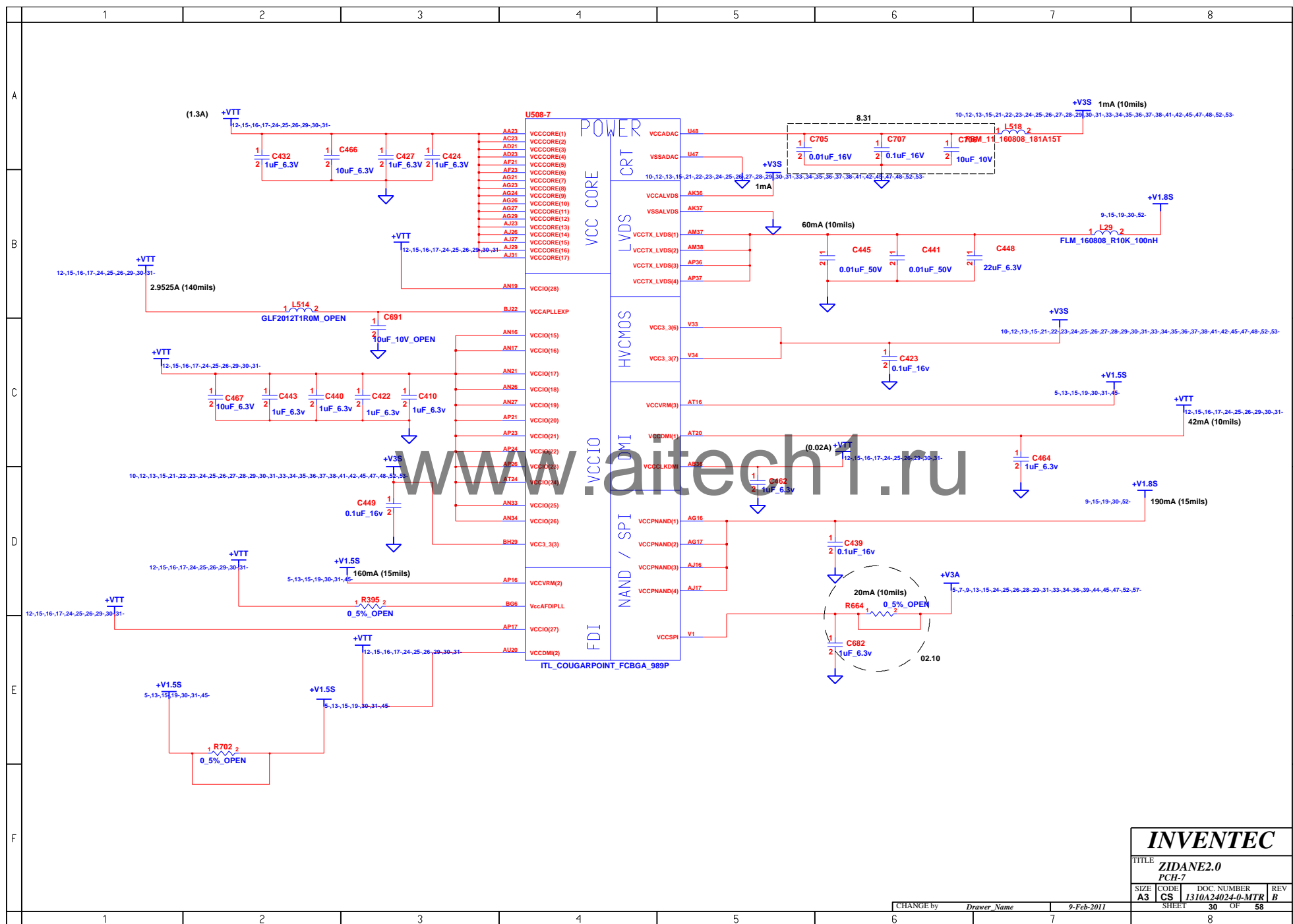
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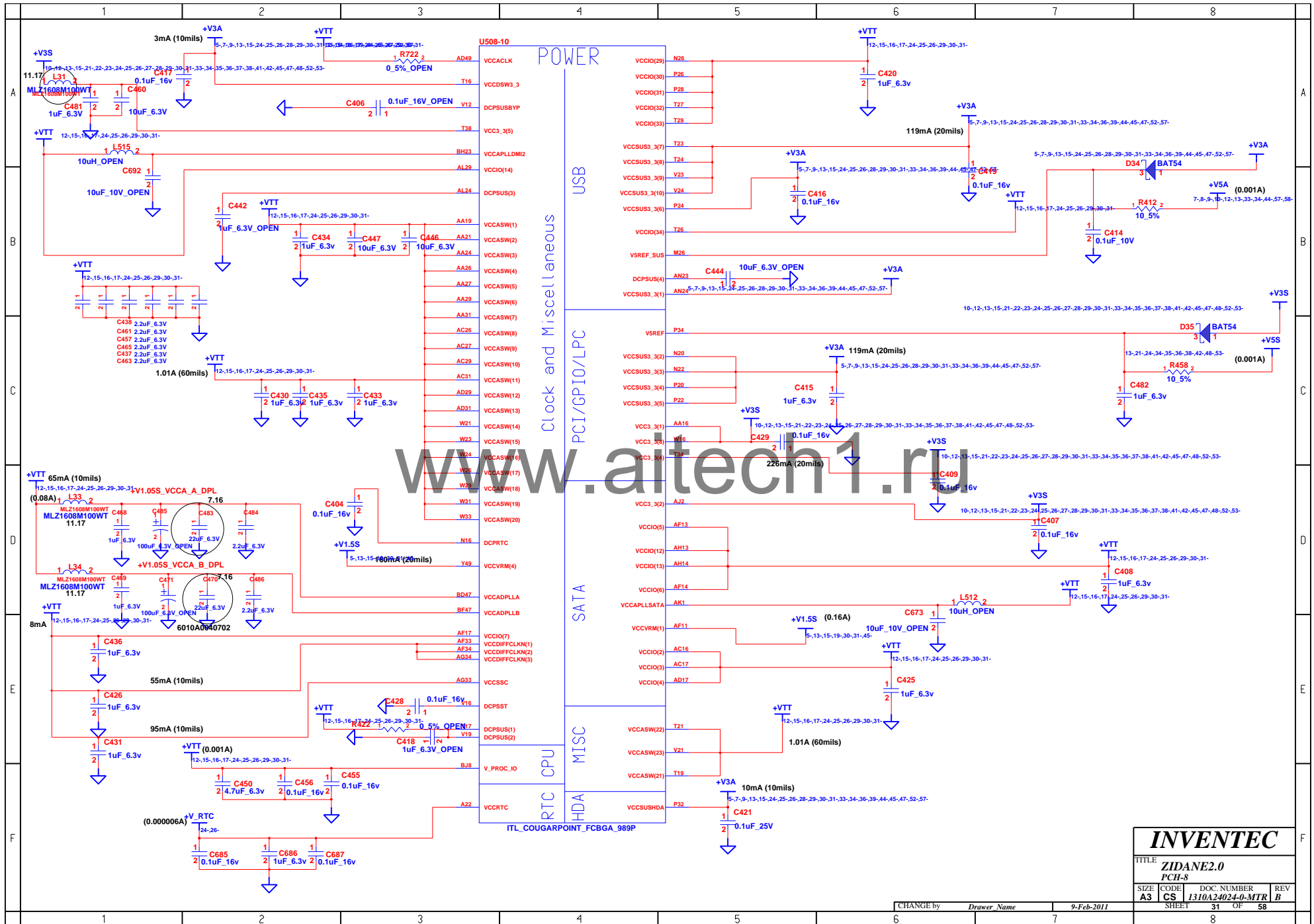


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TITLE			
ZIDANE2.0			
PCH-4			
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SHEET		27	OF 58





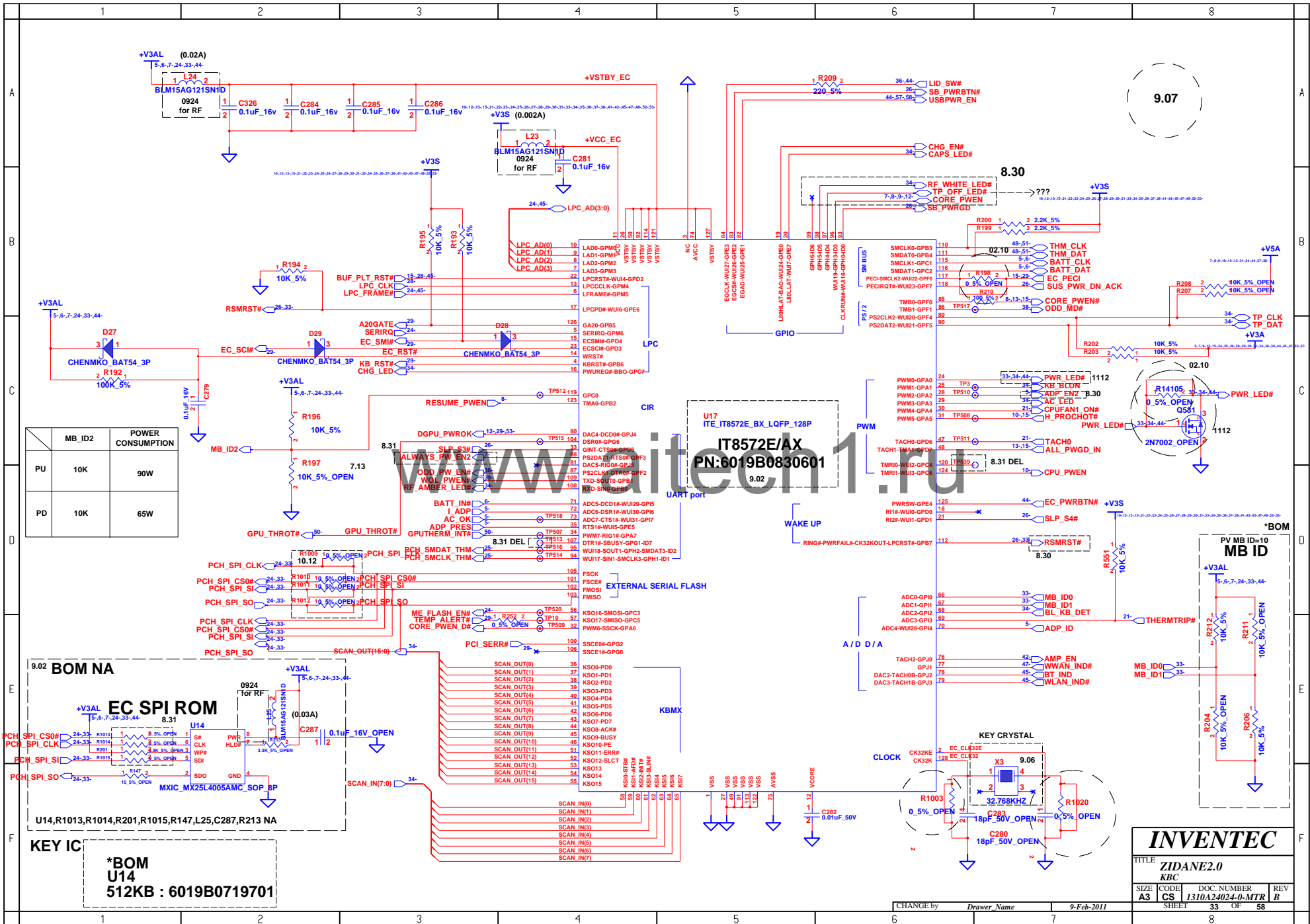




The diagram illustrates the pin connections for two integrated circuits, U508-8 and U508-9, mounted on a PCB. The layout is organized into a grid with letters A-F along the vertical axis and numbers 1-8 along the horizontal axis. U508-8 is located on the left side, and U508-9 is on the right side. Each pin of the ICs is connected to a specific grid location, indicated by red lines and labels. A large watermark 'www.aitech.ir' is overlaid on the center of the diagram. At the bottom right, there is a table with project information:

TITLE			
ZIDANE2.0			
PCH-9			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B
SHEET		32	OF 58





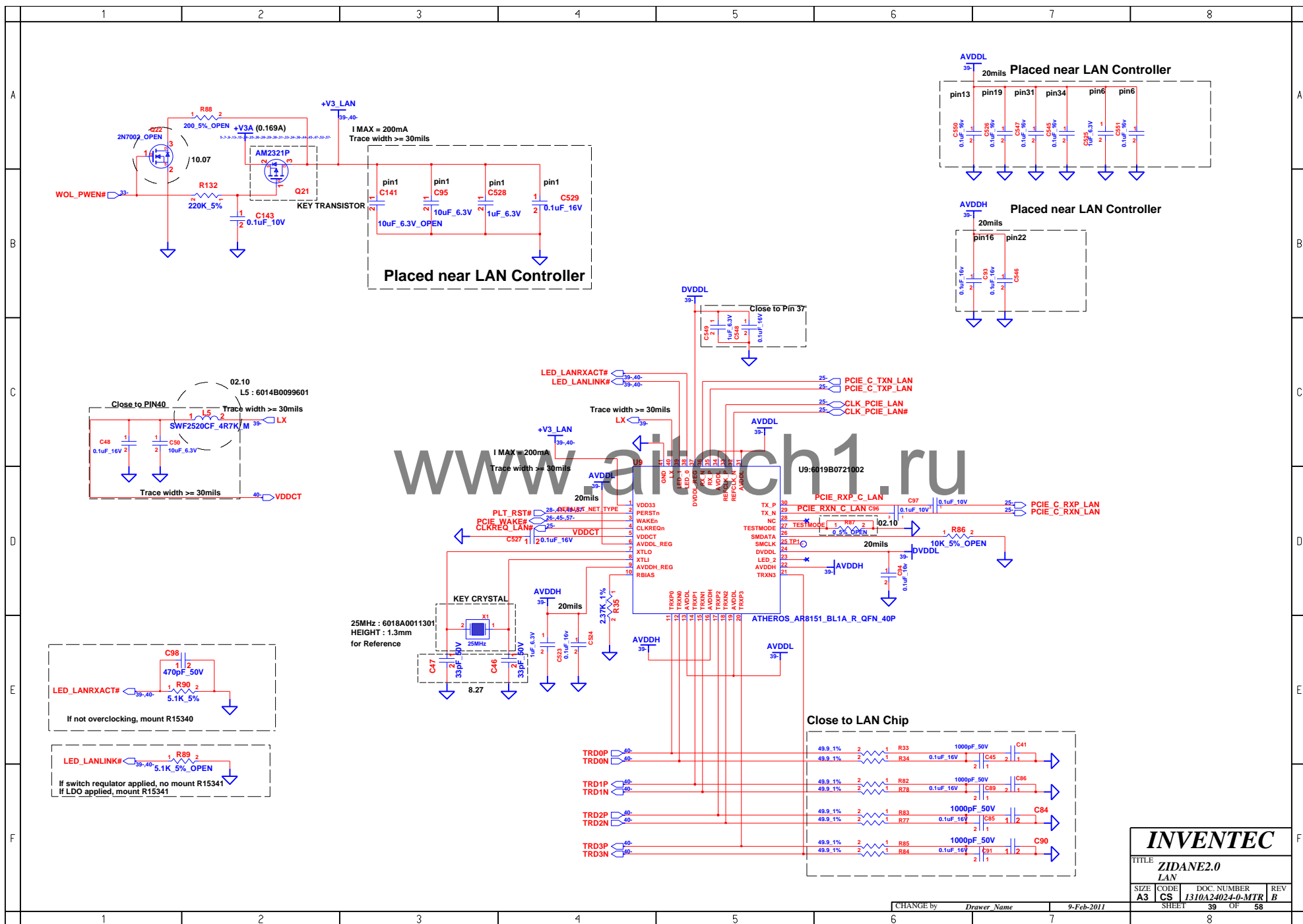


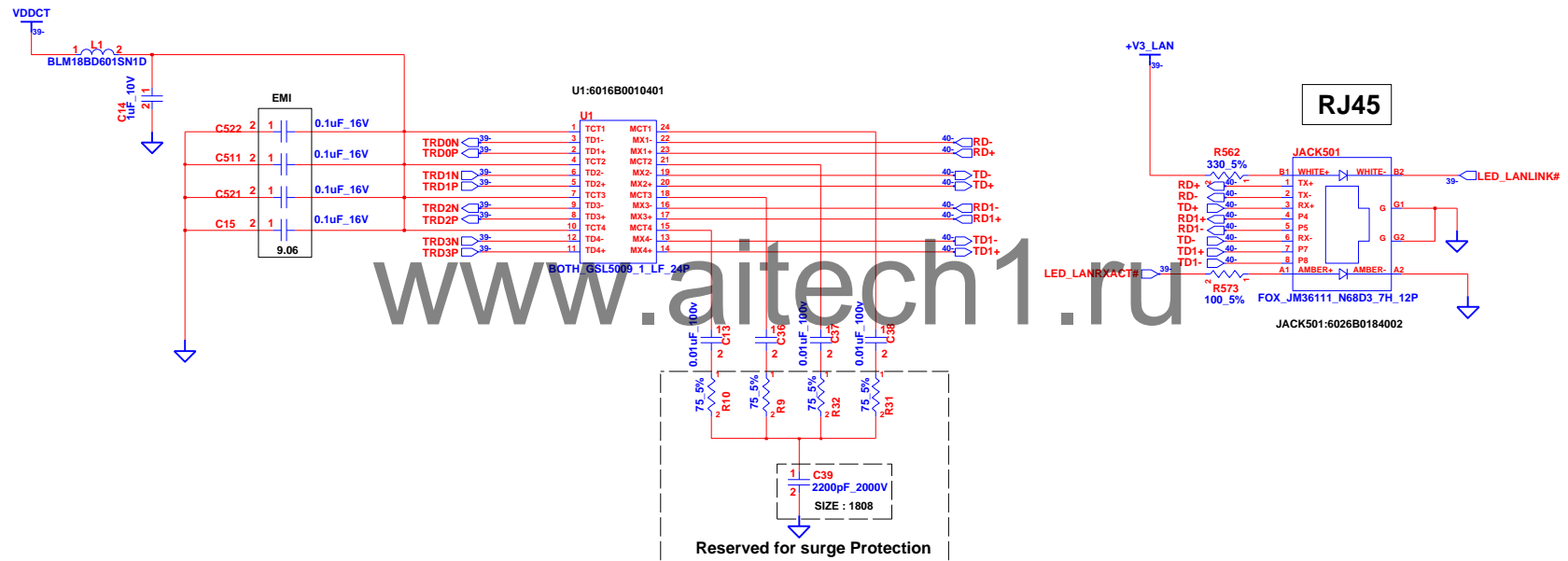












LAYOUT NOTE : Place termination resistors and caps as close to LAN controller as possible

**INVENTEC**

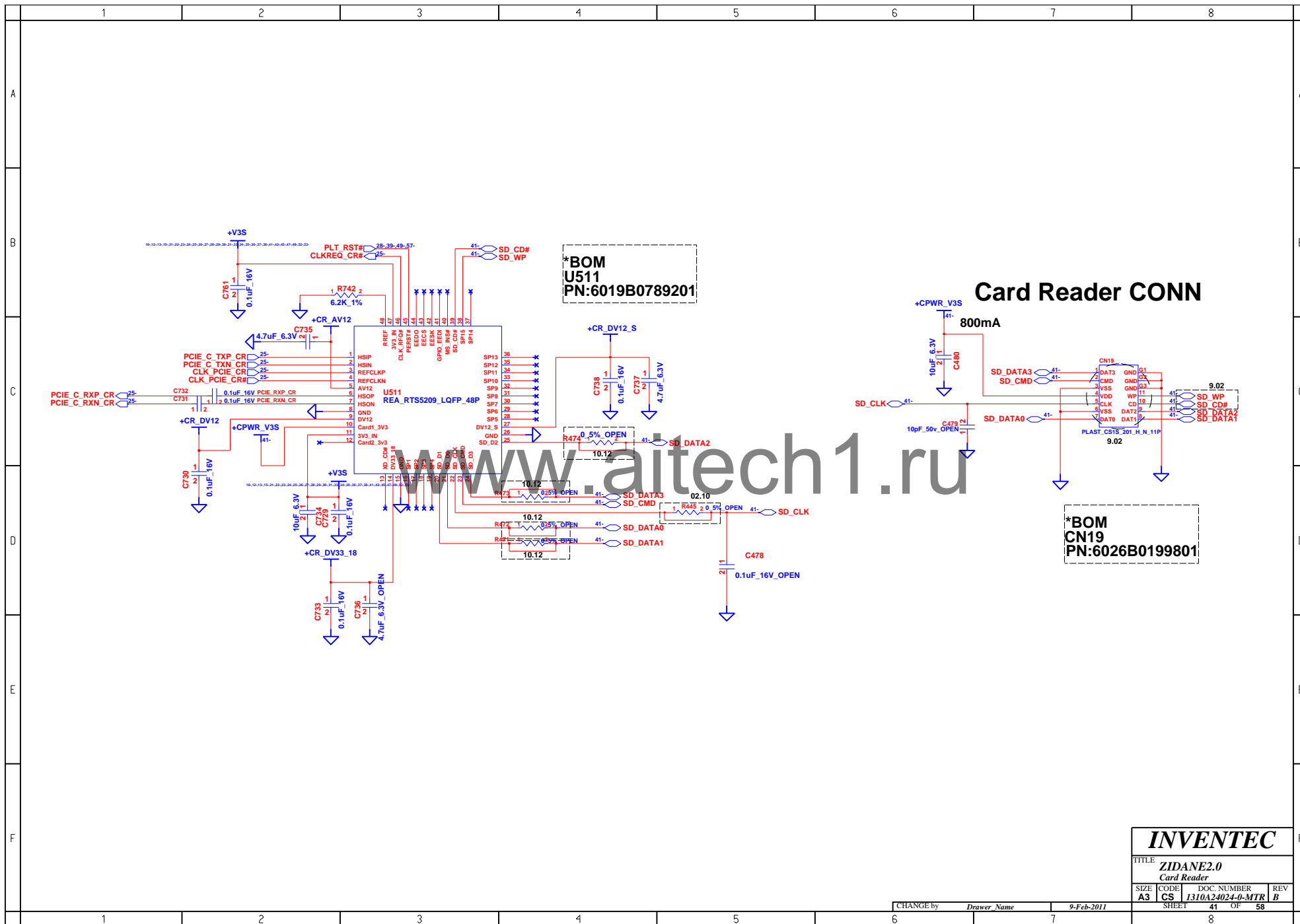
TITLE  
ZIDANE2.0  
RJ-45

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B

CHANGE by *Drawn Name* 9-Feb-2011

SHEET 40 OF 58





**\*BOM**  
**U512**  
**6019B0860701**

**Close to Pin3**  
C723 0.1uF\_16V  
C750 1uF\_6.3V  
C749 0.1uF\_16V  
C722 10uF\_6.3V

**Close to Pin9**  
C723 10uF\_6.3V

**Close to Pin1**  
C742 0.1uF\_16V  
C717 1uF\_10V  
C719 10uF\_10V  
C718 1uF\_10V  
C721 0.1uF\_16V

**Close to Audio Codec**  
C714 2.2uF\_16V  
C715 0.1uF\_10V  
C747 0.01uF\_50V  
C748 0.1uF\_10V  
C746 0.1uF\_10V  
C745 1000pF\_50V  
C744 0.1uF\_10V  
C743 0.1uF\_10V  
C742 0.1uF\_16V  
C741 0.1uF\_16V  
C740 0.1uF\_16V  
C739 0.1uF\_16V  
C738 0.1uF\_16V  
C737 0.1uF\_16V  
C736 0.1uF\_16V  
C735 0.1uF\_16V  
C734 0.1uF\_16V  
C733 0.1uF\_16V  
C732 0.1uF\_16V  
C731 0.1uF\_16V  
C730 0.1uF\_16V  
C729 0.1uF\_16V  
C728 0.1uF\_16V  
C727 0.1uF\_16V  
C726 0.1uF\_16V  
C725 0.1uF\_16V  
C724 0.1uF\_16V  
C723 0.1uF\_16V  
C722 0.1uF\_16V  
C721 0.1uF\_16V  
C720 0.1uF\_16V  
C719 0.1uF\_16V  
C718 0.1uF\_16V  
C717 0.1uF\_16V  
C716 0.1uF\_16V  
C715 0.1uF\_16V  
C714 0.1uF\_16V  
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C693 0.1uF\_16V  
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C518 0.1uF\_16V  
C517 0

**\*BOM**

**U512**

**6019B0860701**

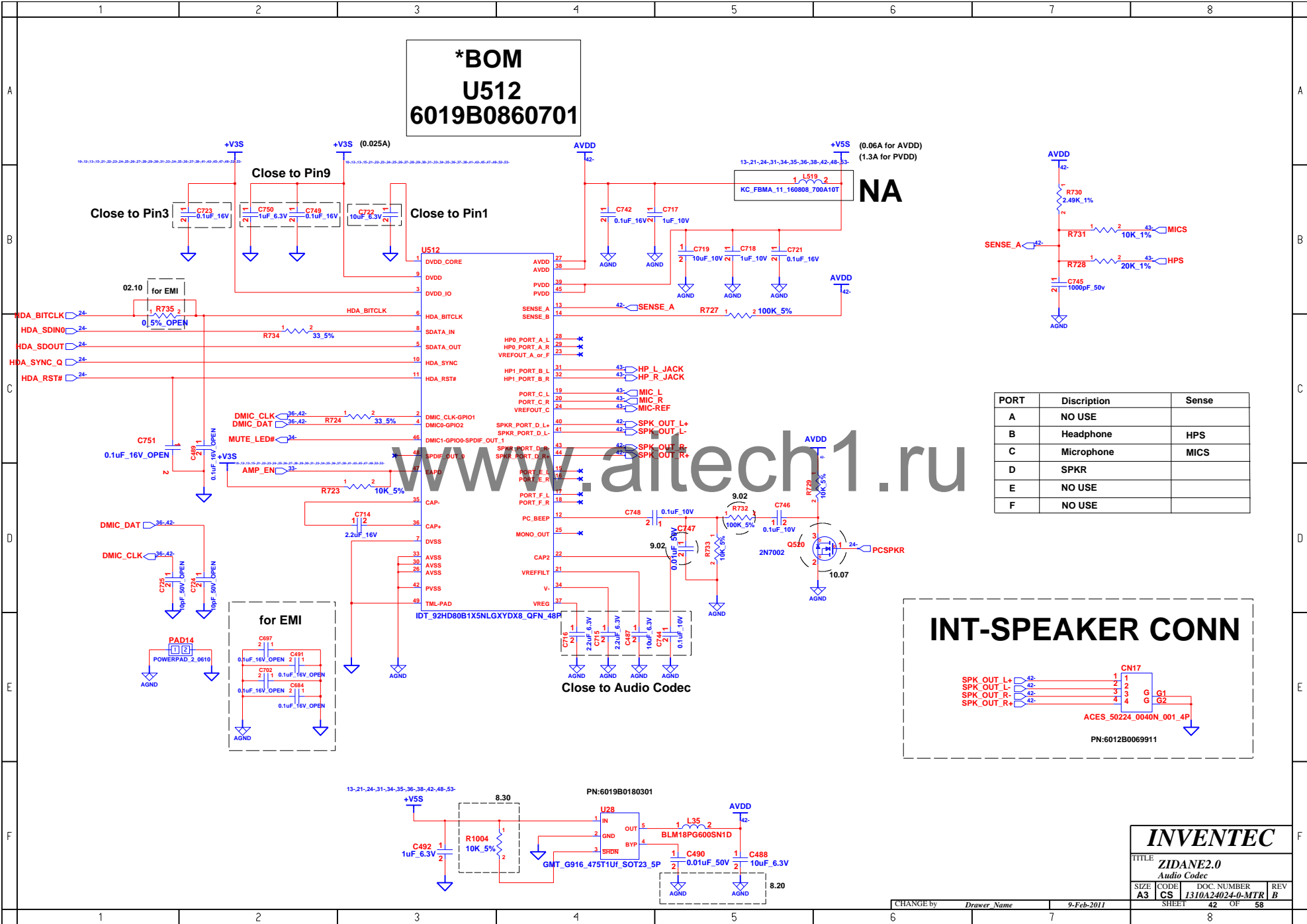
PORT	Discription	Sense
A	NO USE	
B	Headphone	HPS
C	Microphone	MICS
D	SPKR	
E	NO USE	
F	NO USE	

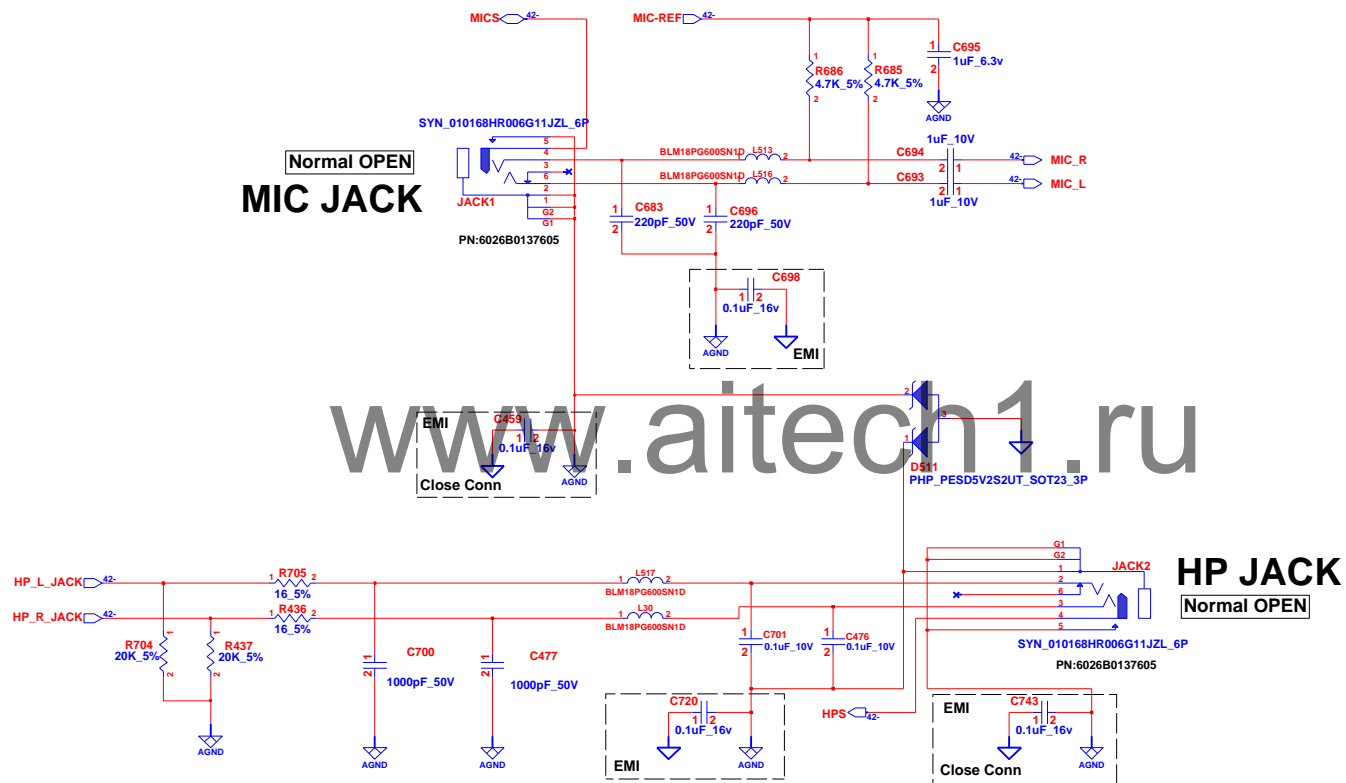
**INT-SPEAKER CONN**

**INVENTEC**

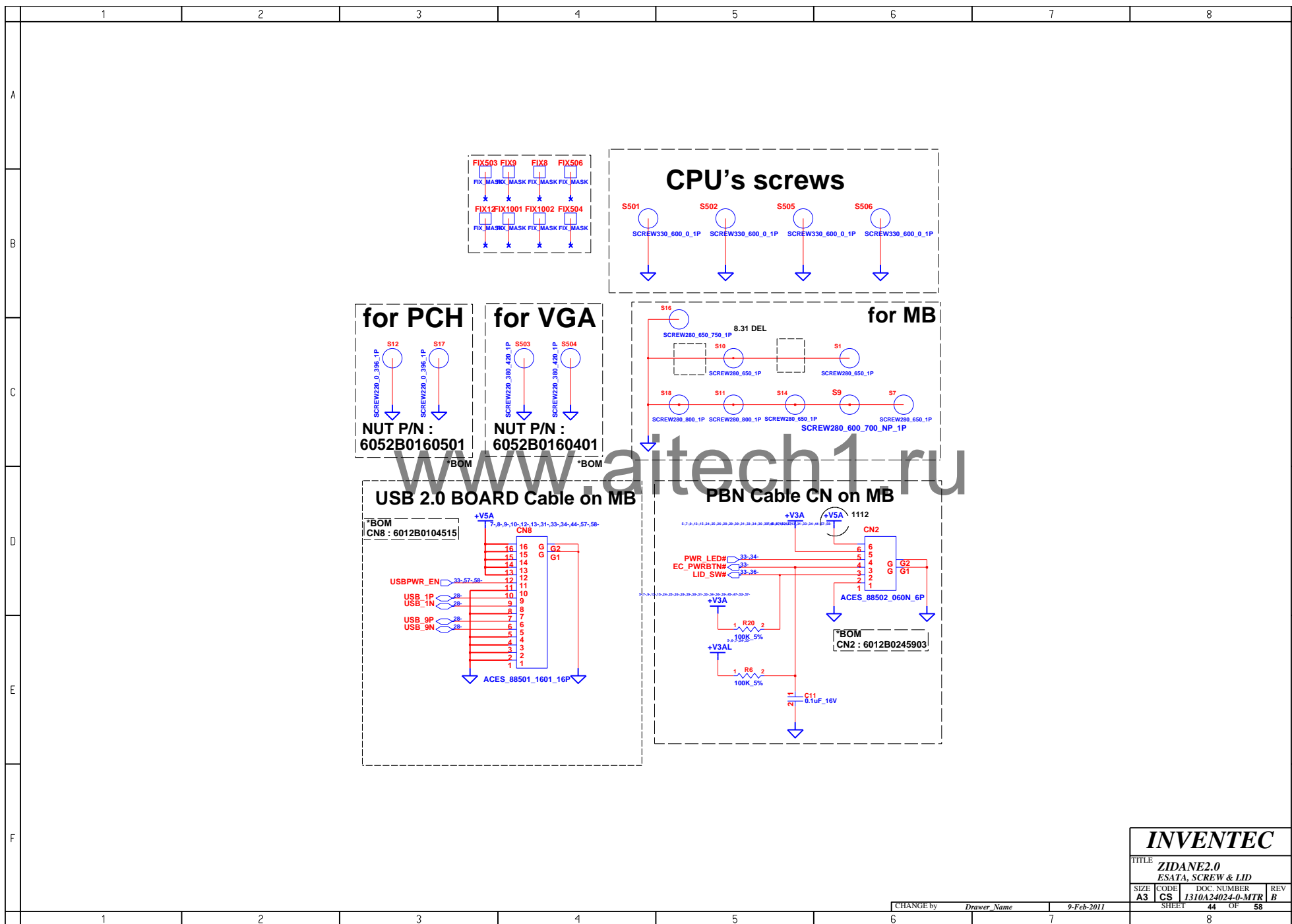
TITLE: ZIDANE2.0  
Audio Codec

SIZE: A3  
CODE: CS  
DOC. NUMBER: I310A24024-0-MTR  
REV: B  
SHEET: 42 OF 58



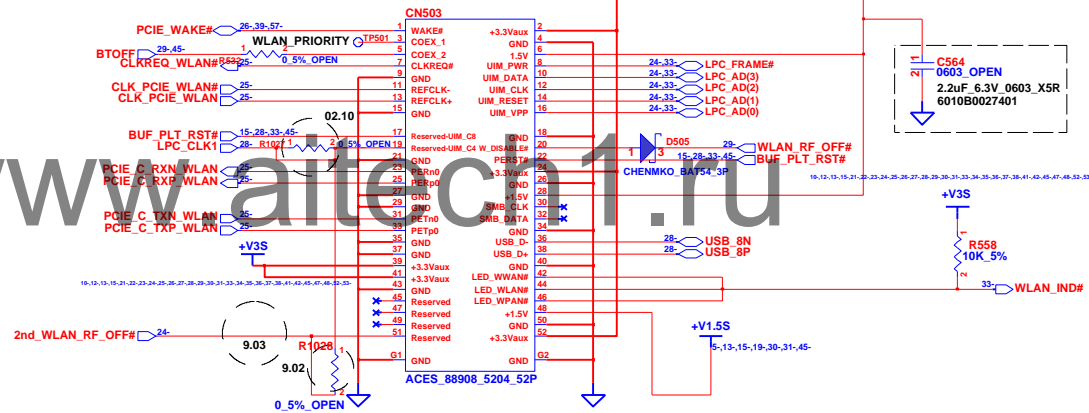
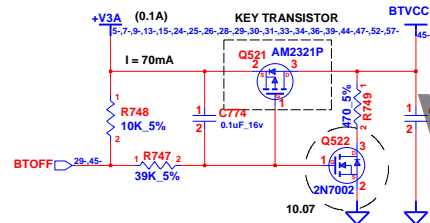


INVENTEC			
TITLE			
ZIDANE2.0			
HP JACK & MIC JACK			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B
CHANGE by		Drawer Name	9-Feb-2011
SHEET		43	OF 58



INVENTEC			
TITLE			
ZIDANE2.0			
ESATA, SCREW & LID			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B
CHANGE by		Drawer Name	9-Feb-2011
SHEET		44	OF 58

## WLAN CONN (MINICARD)



**P/N:6026B0184301**

<b>INVENTEC</b>			
TITLE <b>ZIDANE2.0</b> <i>WLAN, BT &amp; WebCAM</i>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>I310A24024-0-MTR</i>	REV <b>B</b>
SHEET		45 OF	58

## A



## C



## F



1



for Dauther Board

A

1

C

C

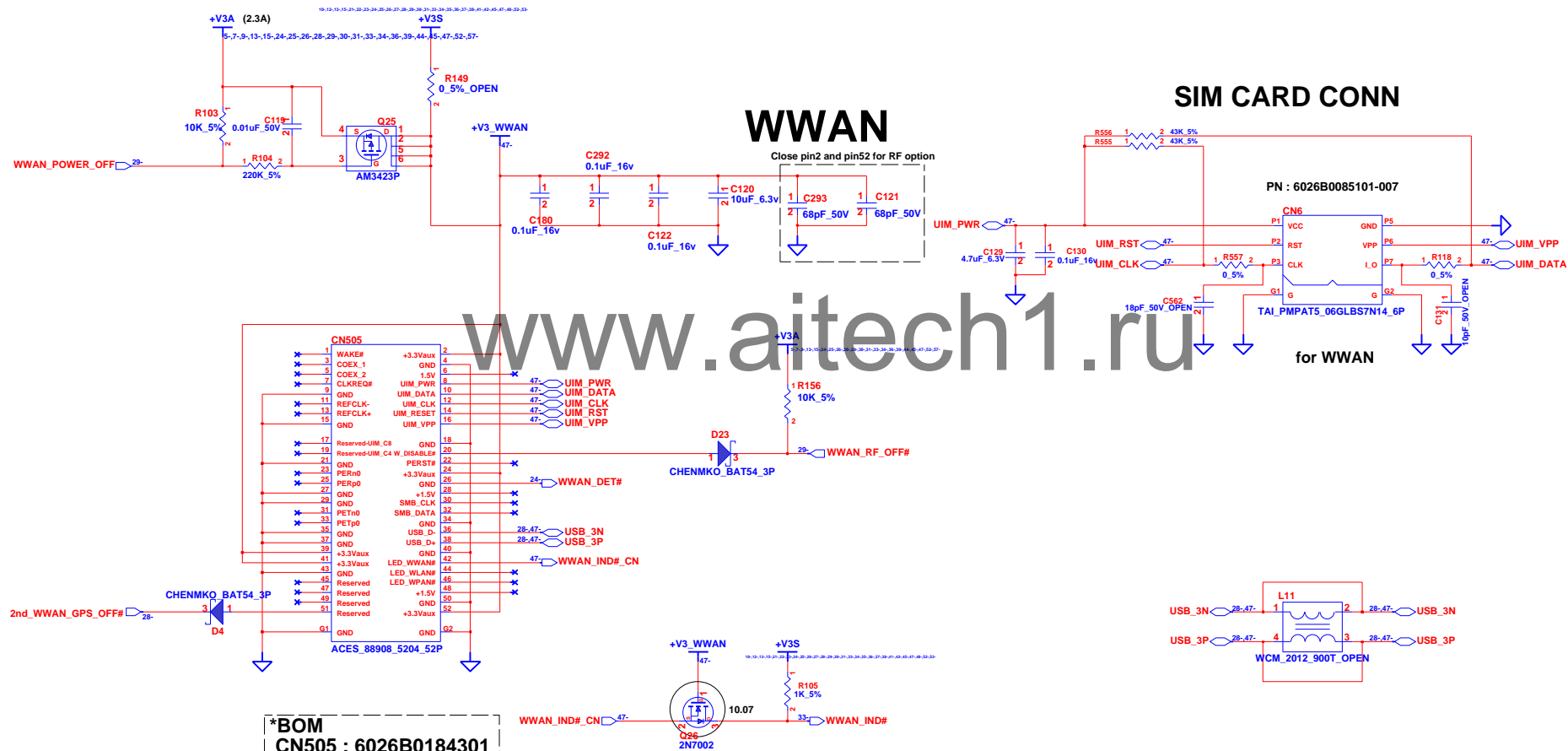
1

1

TITLE				
<b>ZIDANE2.0</b> <i>USB, PowerButton (DB)</i>				
SIZE	CODE	DOC. NUMBER		REV
<b>A3</b>	<b>CS</b>	<b>1310A24024-0-MTR</b>		<b>B</b>
SHEET		46 OF 58		

CHANGE by	<i>Drawer Name</i>	<i>9-Feb-2011</i>
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# OPTION PART



\*BOM  
CN505 : 6026B0184301

**INVENTEC**

TITLE: ZIDANE2.0  
WWAN(Optional)

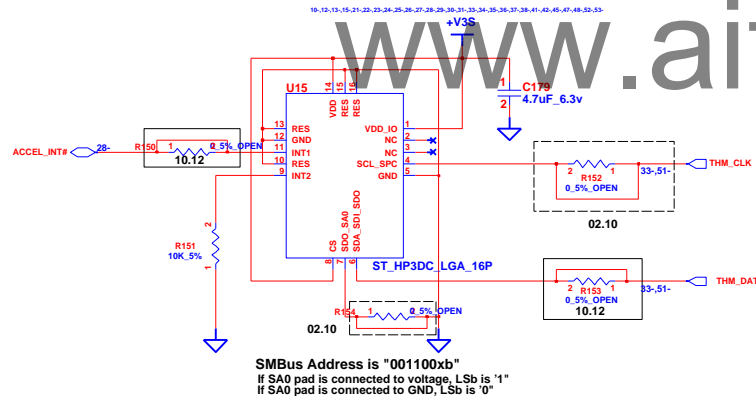
SIZE: A3 CODE: CS DOC. NUMBER: 1310A24024-0-MTR REV: B

CHANGE by: Drawer Name 9-Feb-2011

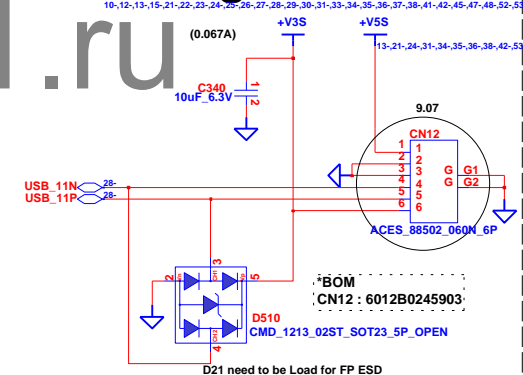
SHEET 47 OF 58

# OPTION PART

## HARDDRIVE PROTECTION



## FingerPrint



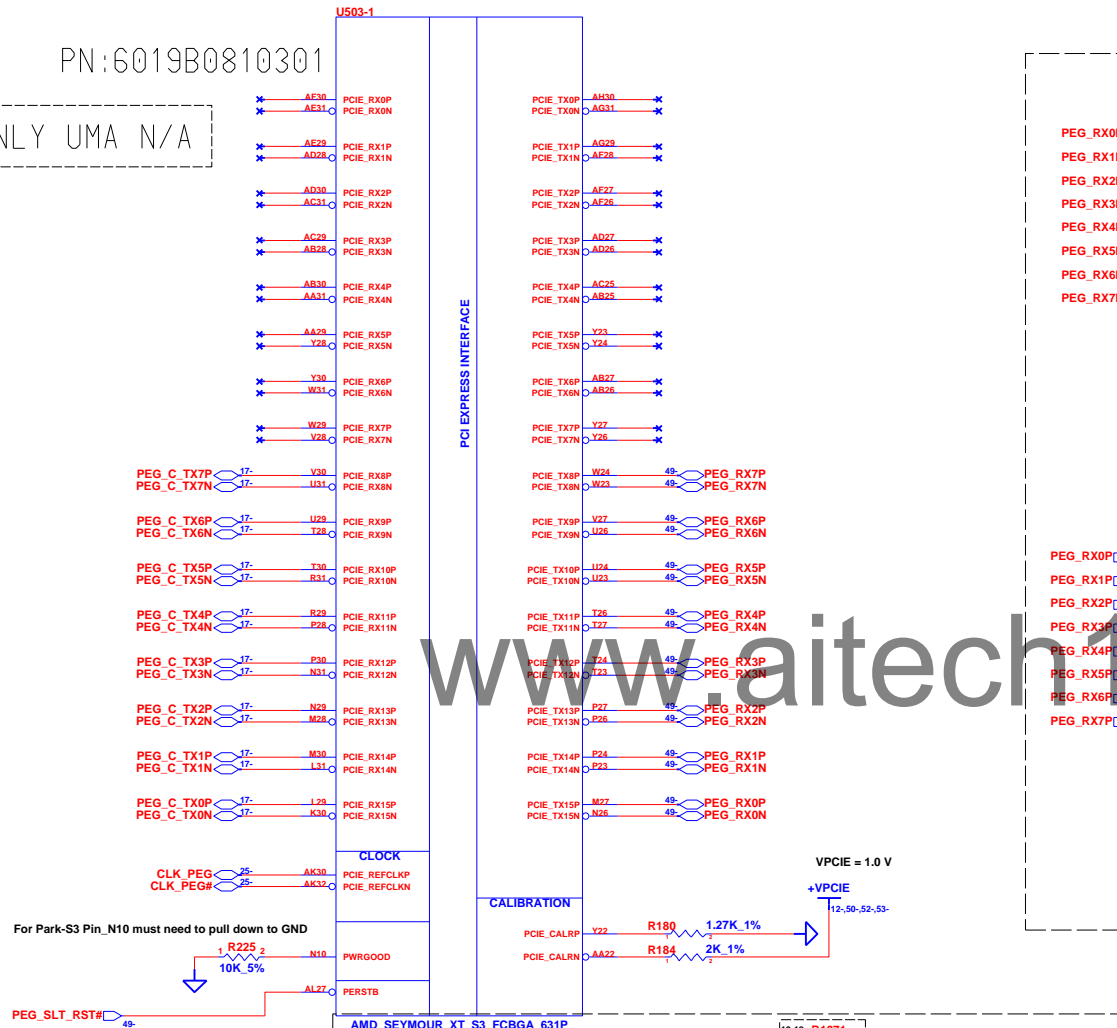
INVENTEC			
TITLE: ZIDANE2.0			
Touchscreen, FP & HD LOCK(Option)			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A24024-0-MTR	REV: B
SHEET: 48		OF: 58	

CHANGE by: *Drawer Name* 9-Feb-2011

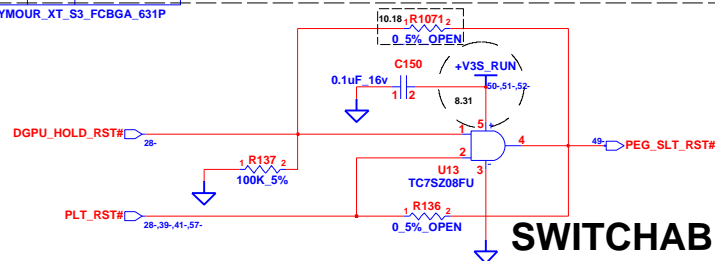
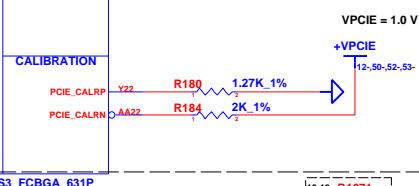
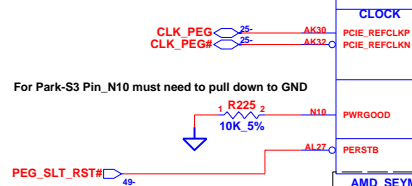
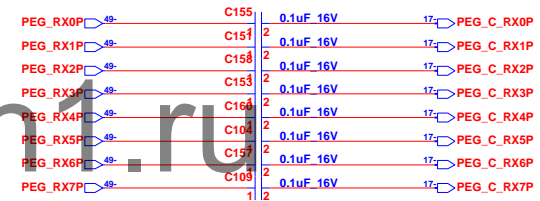
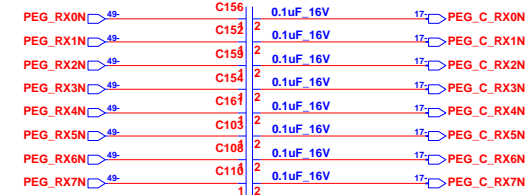


PN:6019B0810301

DIS ONLY UMA N/A



## Close to GPU



**INVENTEC**

TITLE  
ZIDANE2.0

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B

CHANGE by: Drawer Name 9-Feb-2011

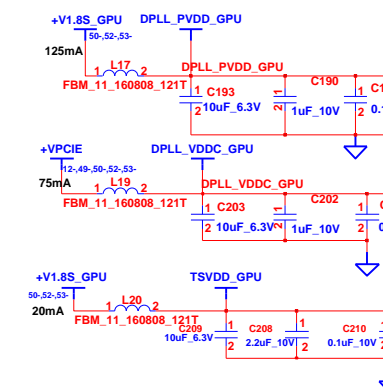
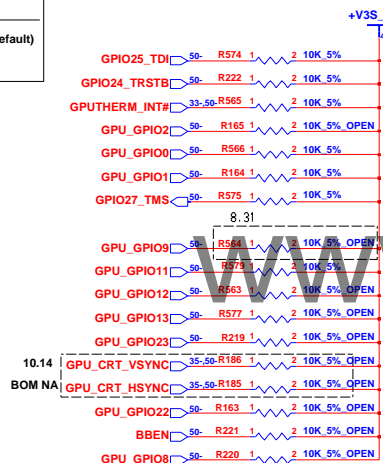
SHEET 49 OF 58

(Default)

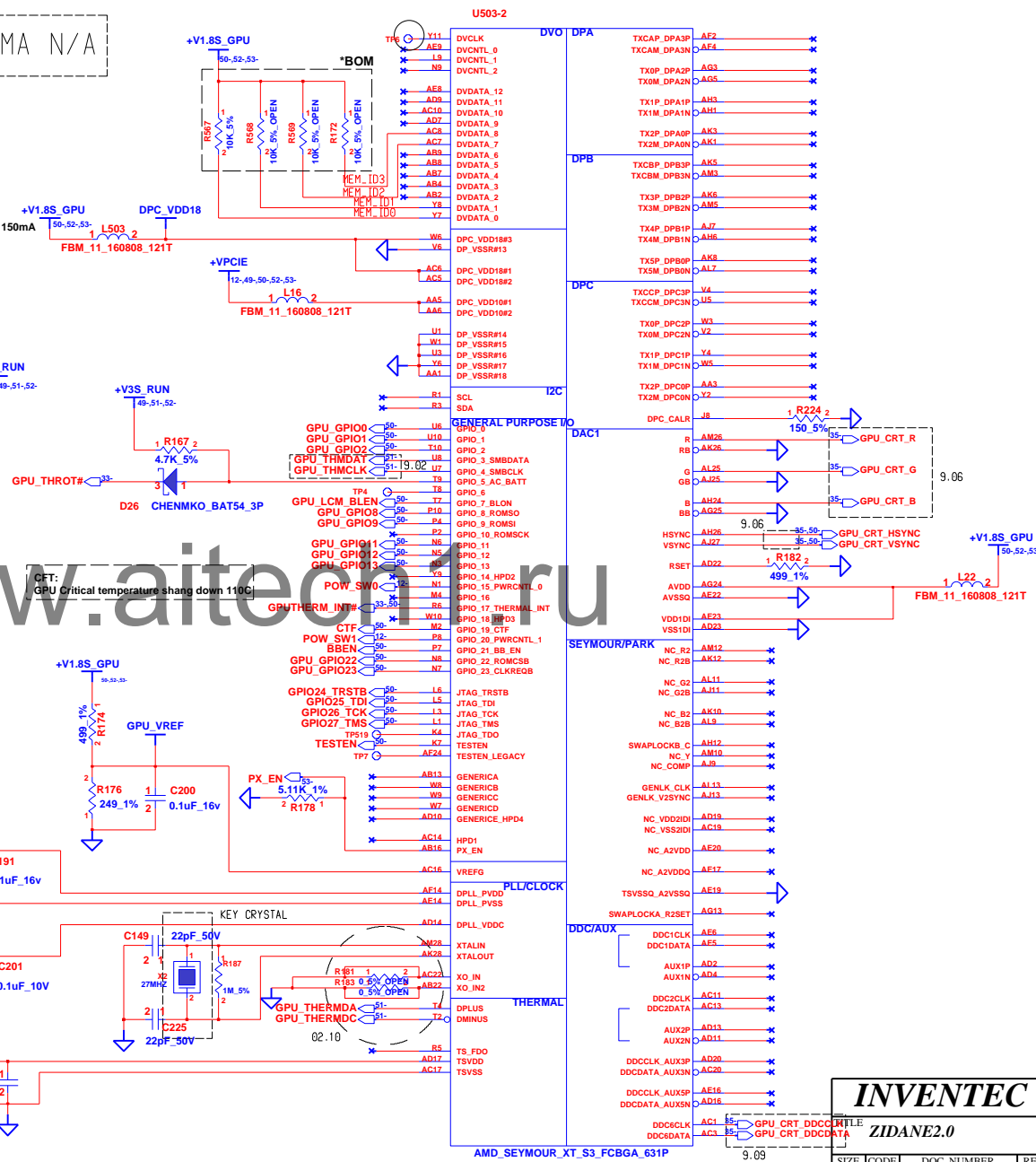
DIS ONLY UMA N/A

110mA

If GPIO\_22\_EN = 0, then GPIO[13:11] defines the primary memory aperture size.

19

POW_SW1	POW_SW0	+VDDC_GPU
0	0	1.1V
0	1	1V
1	0	0.95V
1	1	0.9V



**INVENTEC**

**TITLE** ZIDANE2.0

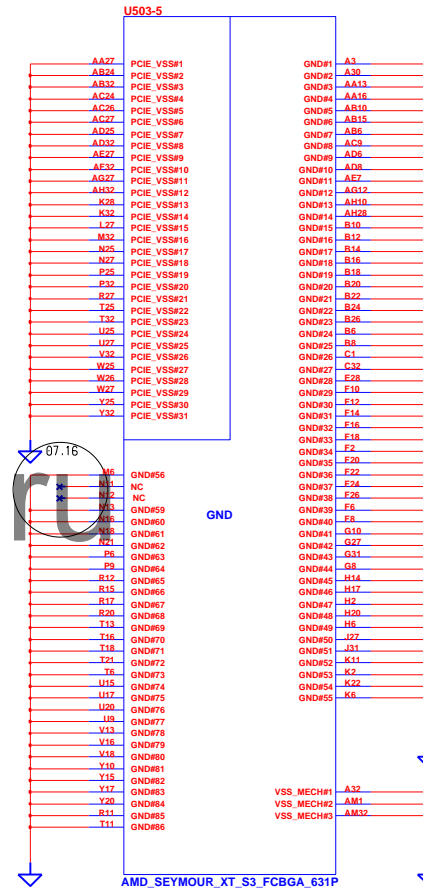
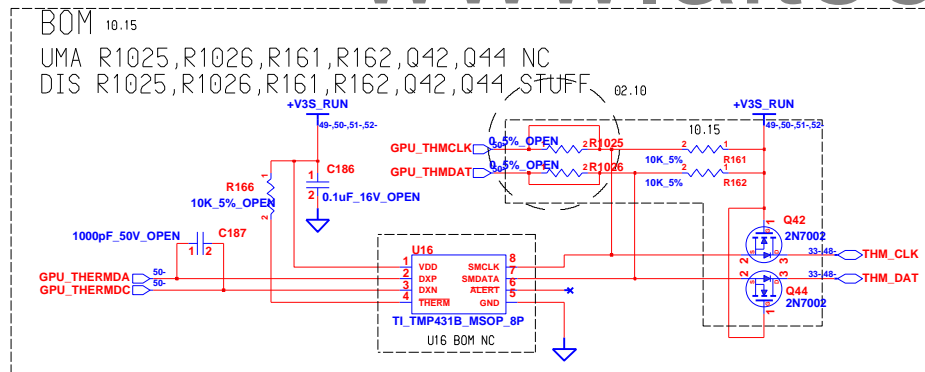
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>1310A24024-0-MTR</i>	RE <i>B</i>
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DIS ONLY UMA N/A

KEY IC

\*BOM  
U16

PN: 6019B0437702



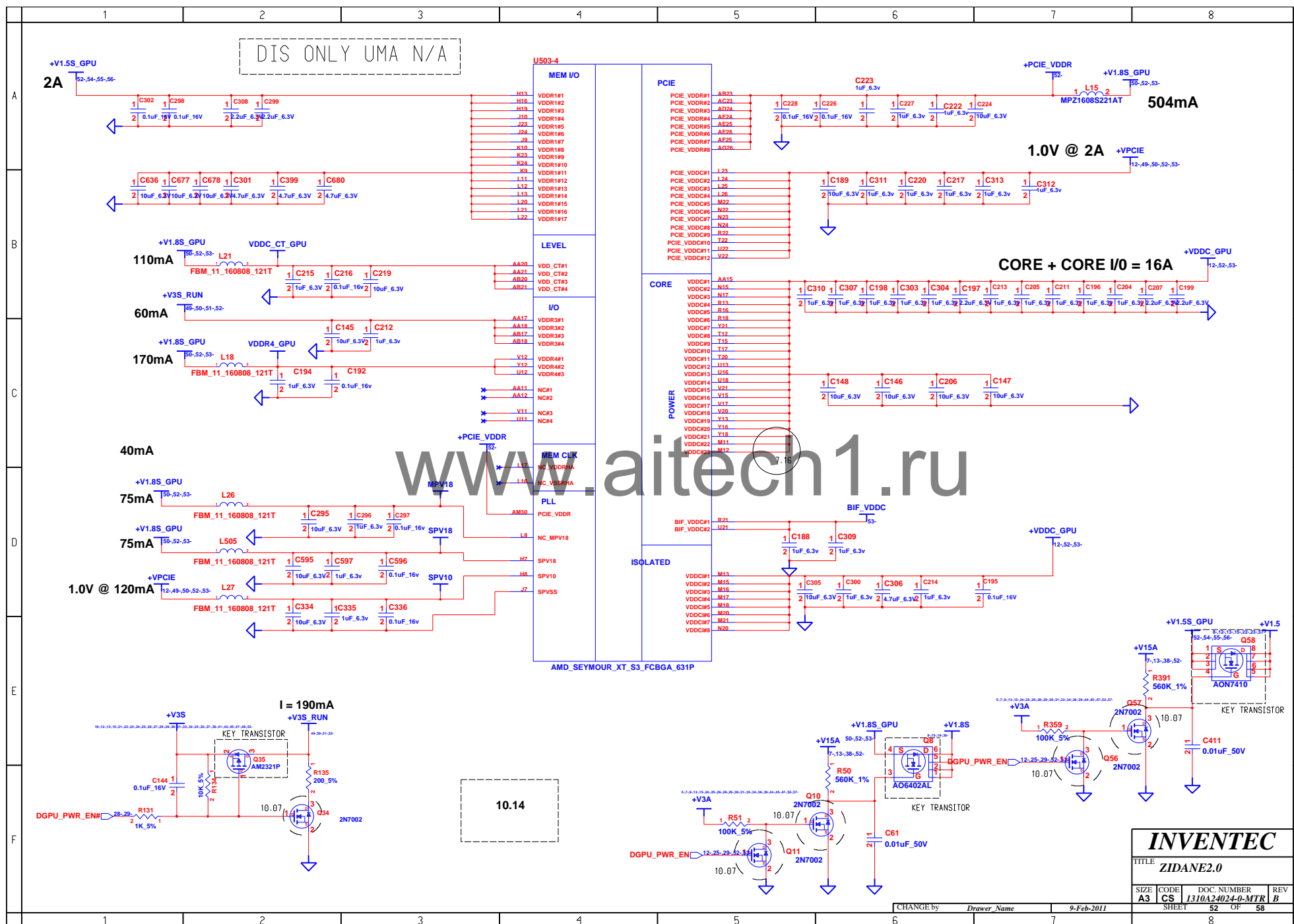
INVENTEC

TITLE  
ZIDANE2.0

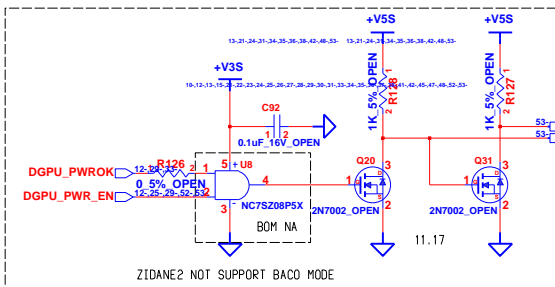
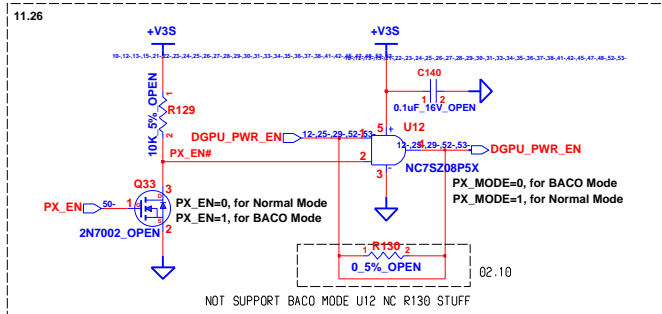
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B

CHANGE by: Drawer Name 9-Feb-2011

SHEET 51 OF 58

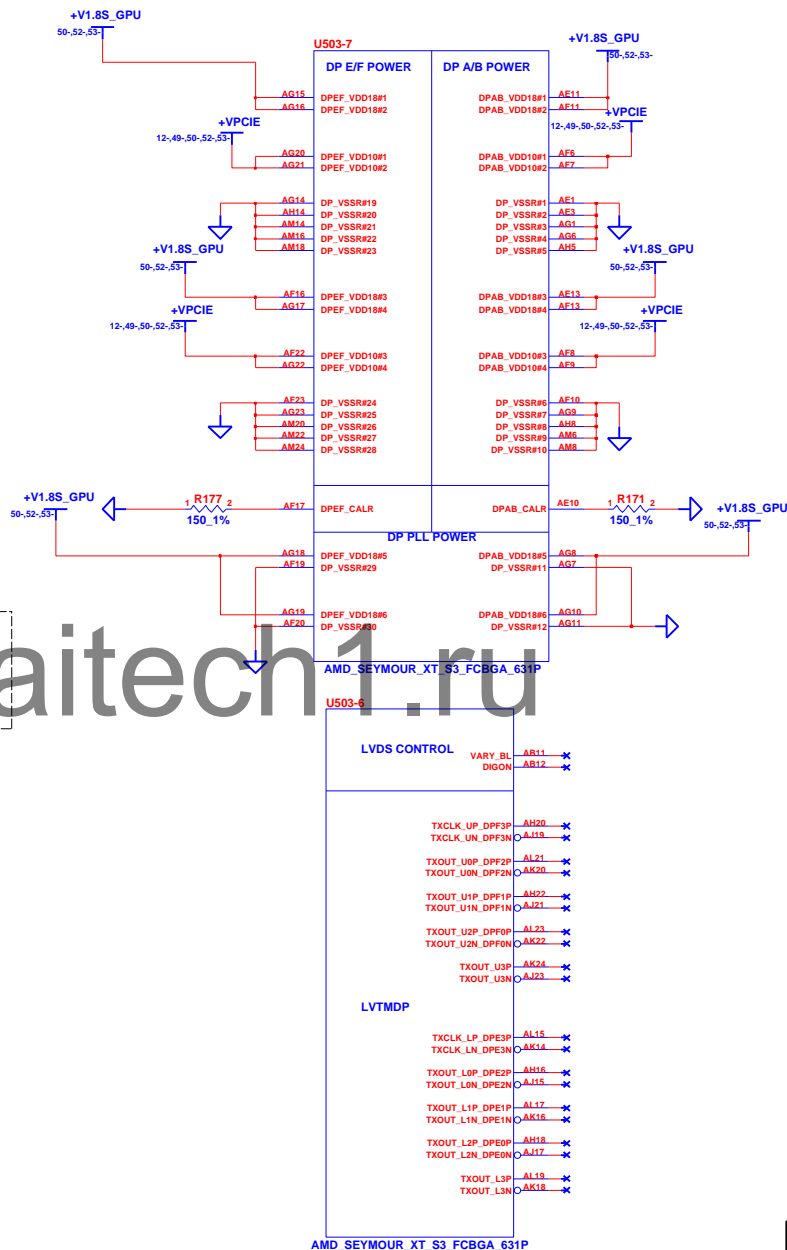
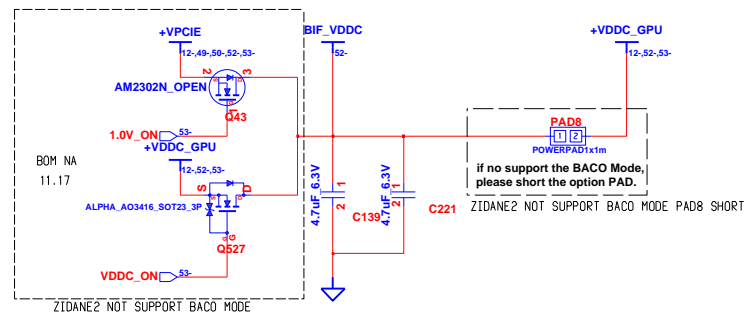


DIS ONLY UMA N/A  
MV BUILD NEED TO MODIFY THE R130



U8&U12 NA

\*BOM  
U8&U12  
PIN: 6019A0059801



INVENTEC

TITLE  
ZIDANE2.0

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B

CHANGE by Drawer Name 9-Feb-2011

SHEET 53 OF 58

DIS ONLY UMA N/A

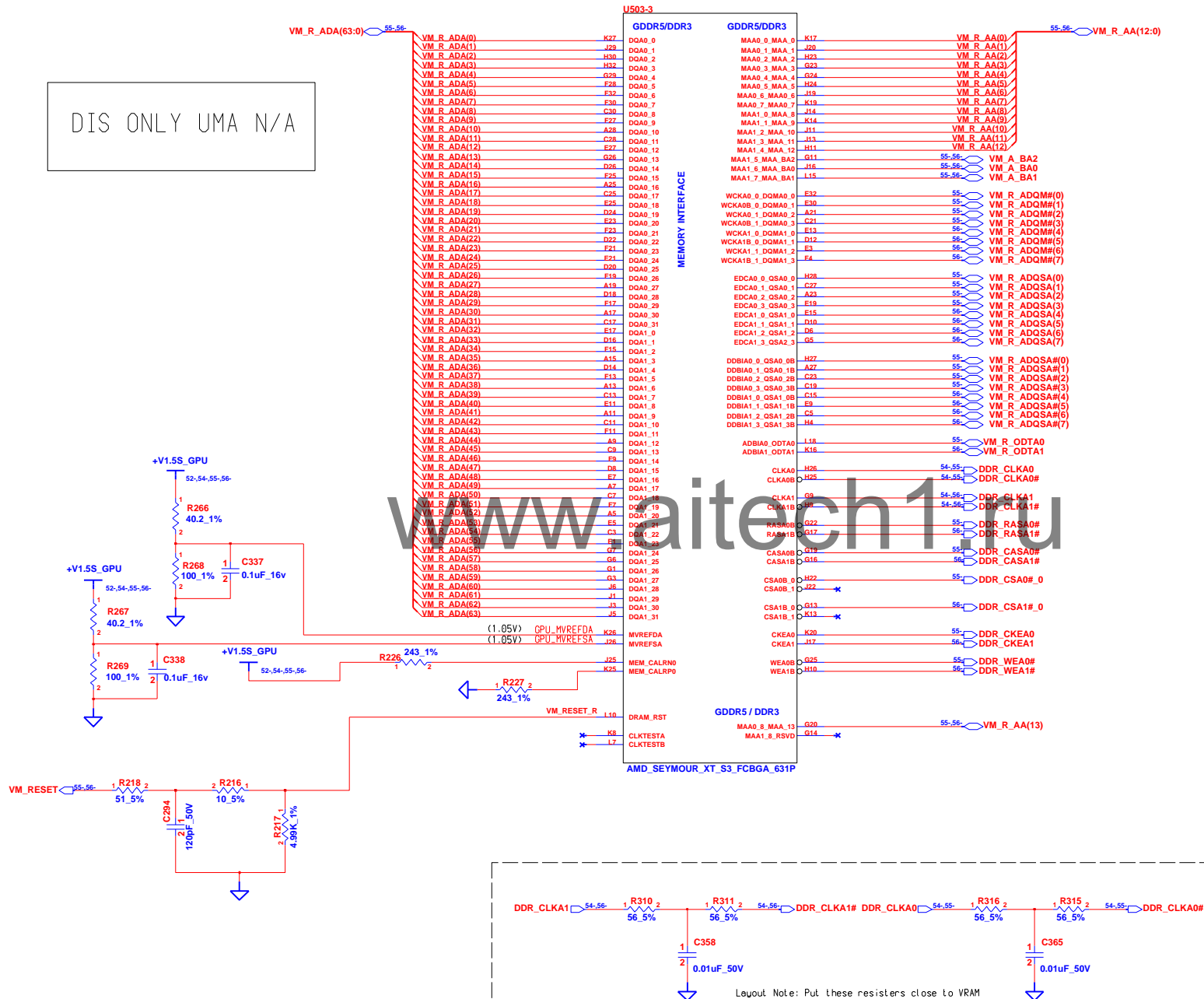
www.aitech1.com

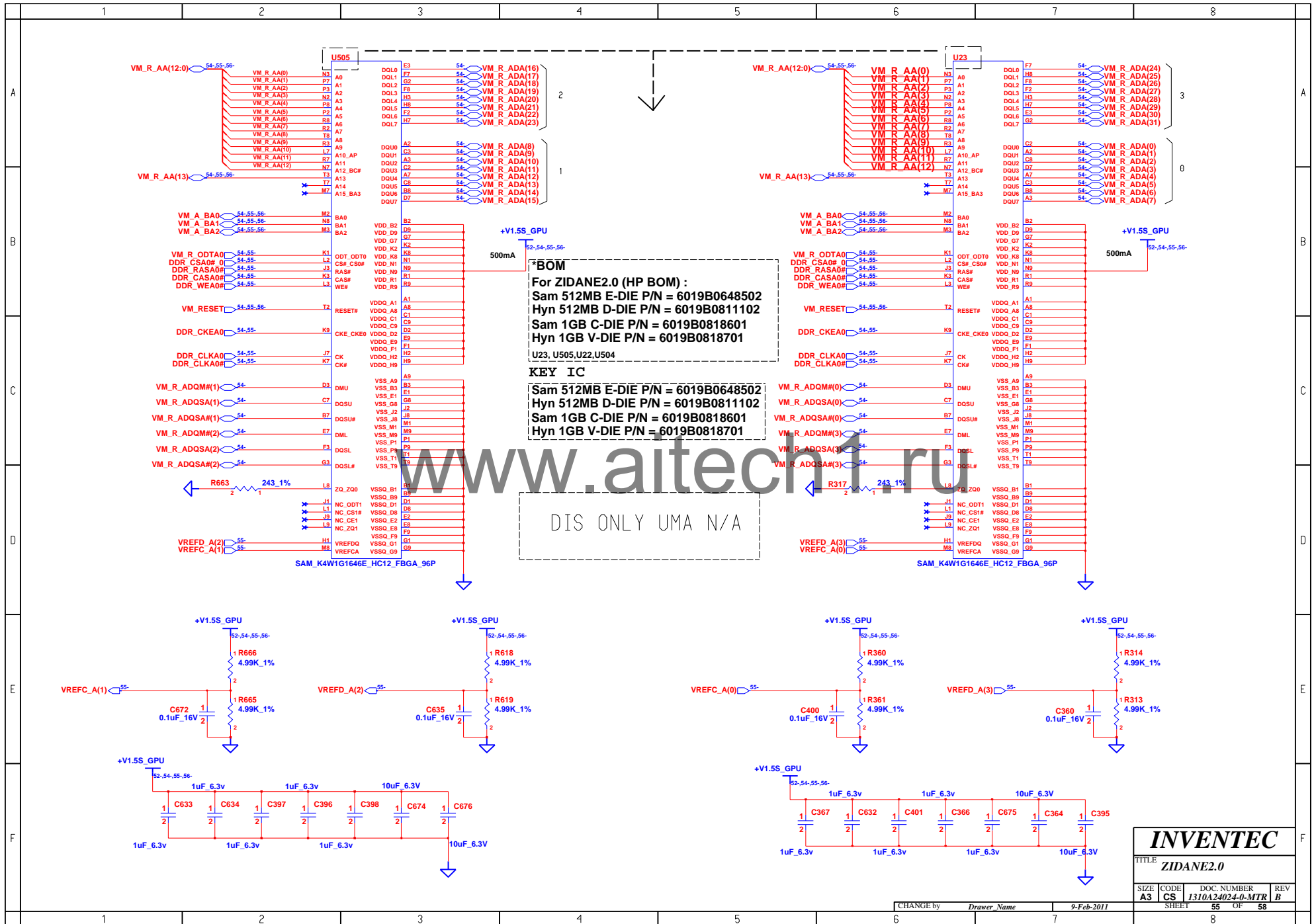
INVENTEC

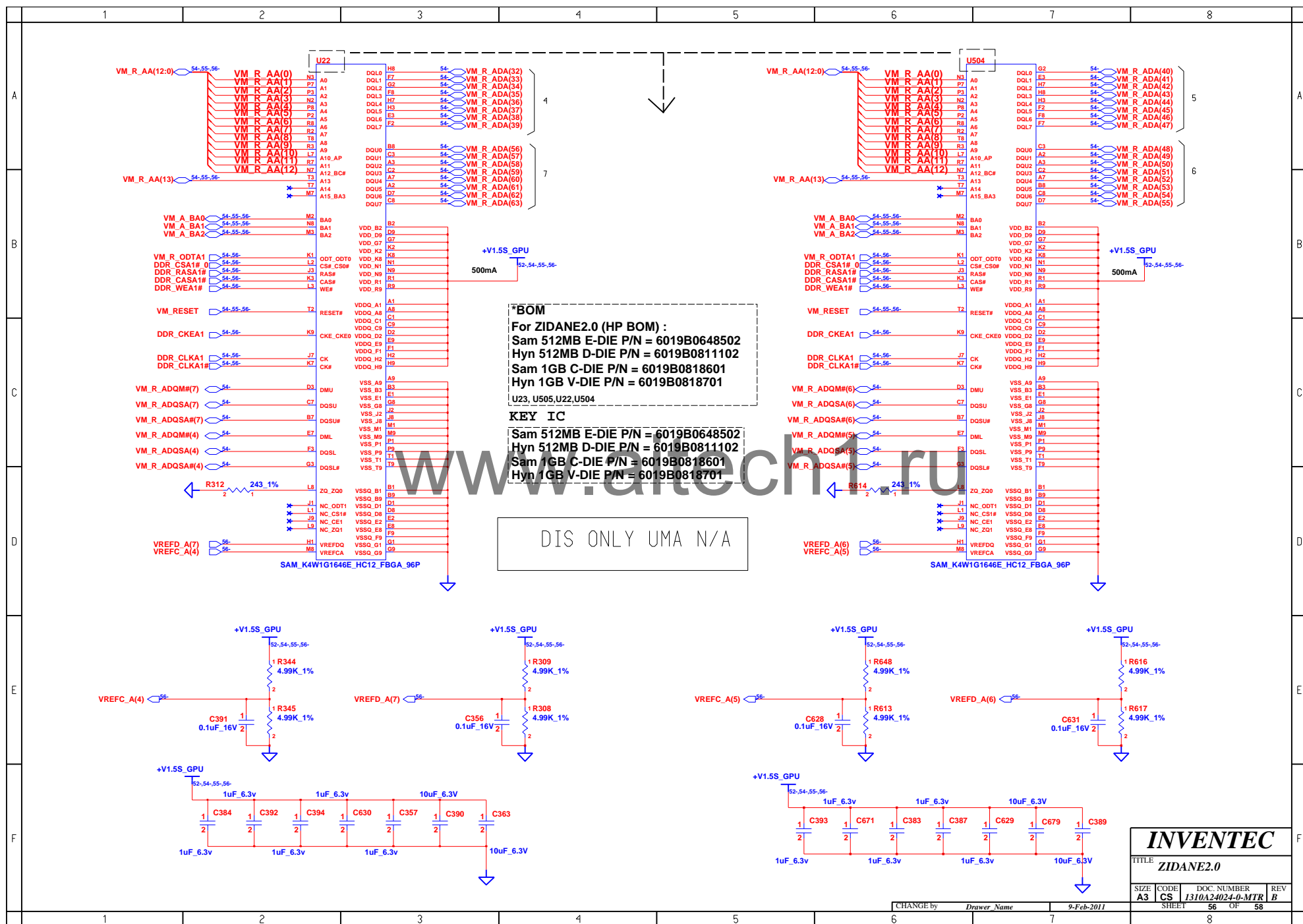
TITLE  
ZIDANE2.0

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24024-0-MTR	B
SHEET		54	OF 58

CHANGE by *Drawer Name* 9-Feb-2011



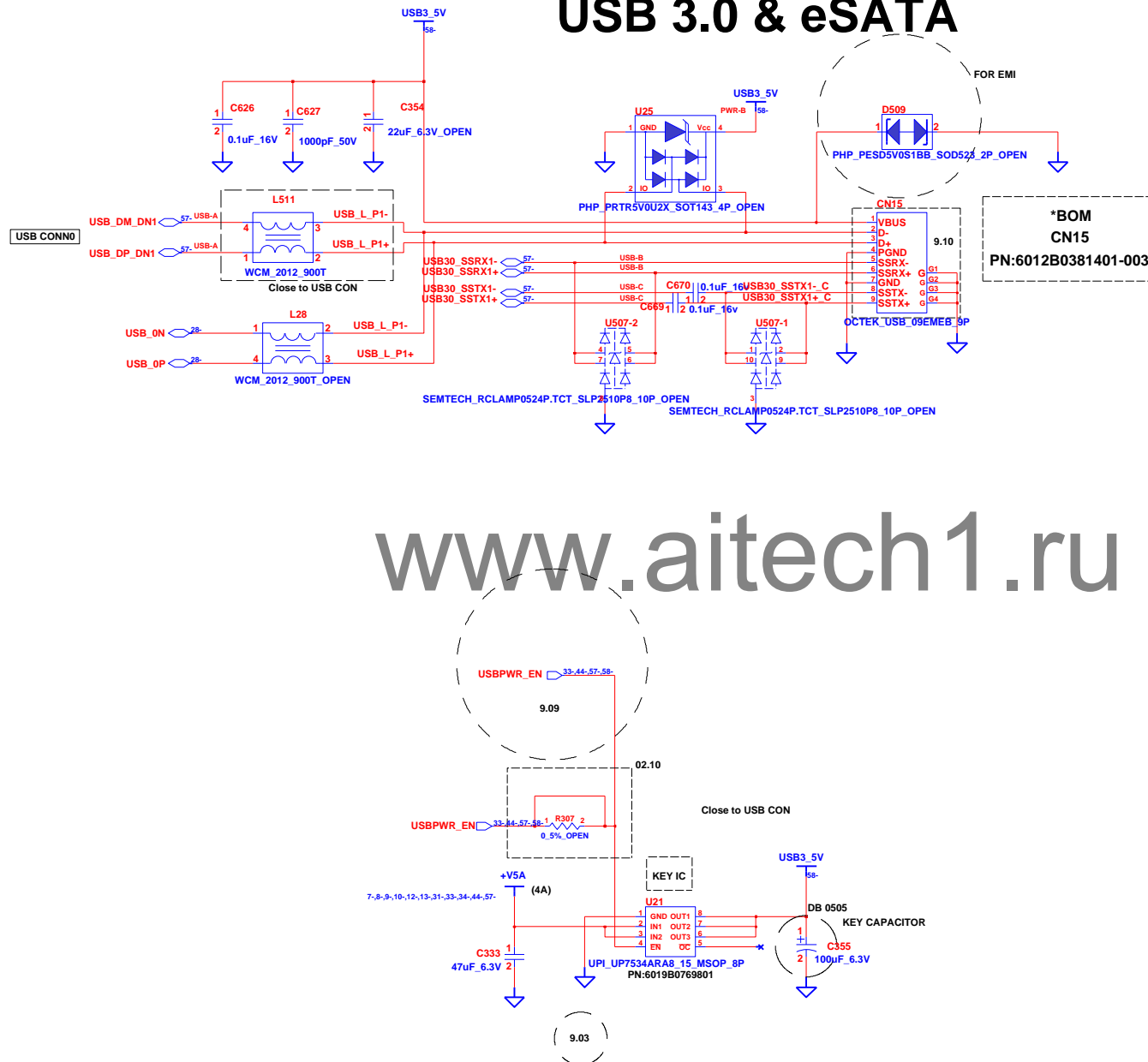








# USB 3.0 & eSATA



INVENTEC			
TITLE ZIDANE2.0			
SIZE A3	CODE CS	DOC. NUMBER 1310A24024-0-MTR	REV B
CHANGE by Drawer Name		9-Feb-2011	
SHEET		58	OF 58